BL616/BL618

数据手册

Version: 2.5

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Features

- 无线（业内顶尖射频性能）
  - 2.4 GHz 射频收发器
  - Wi-Fi 6 (IEEE 802.11 b/g/n/ax)
  - 蓝牙 ® 5.3 双模 (BT+BLE)
  - IEEE 802.15.4(Zigbee/Thread)
  - 支持 BLE 的 Wi-Fi 快速连接
  - Wi-Fi/蓝牙/802.15.4 共存
  - Wi-Fi 安全 WPS/WEP/WPA/WPA2/WPA3
  - Wi-Fi 20/40MHz 带宽，1T1R，高达 229.4 Mbps
  - 支持 LDPC、STBC、Beamformee、DL/UL OFDMA、MU-MIMO、TWT（目标唤醒时间）、SR（空分复用）、DCM（双载波调制）、ER（扩展范围）
  - 支持聚合（AMPDU、AMSDU）、立即块确认、分片和碎片整理
  - 支持 RX 分集
  - 支持 IEEE 802.11e QoS WMM（Wi-Fi 多媒体）、IEEE 802.11w PMF（管理帧保护）
  - STA、SoftAP、STA+SoftAP 和 sniffer 模式
  - 多云连接
  - 集成射频 balun、PA/LNA
  - 支持外部 PA/LNA
- 微控制器子系统
  - 带 FPU 和 DSP 的 32 位 RISC-V CPU
  - 一级缓存
  - RTC 定时器最长计数周期为 1 年
  - 2 个 32 位通用定时器
  - 4 个 DMA 通道
  - 动态频率可配置为 1MHz 至 320MHz
  - JTAG 开发支持
  - 支持 NOR FLASH XIP
- 音频编码译码器 (仅在 BL618 支持)
  - Audio ADC*1 (MIC, SNR>92dB)
  - Audio DAC*1 (Speaker, SNR>95dB)
  - 支持 8/12/16/22.05/24/32/44.1/48KHz
- Memory
  - 532KB SRAM[1]
  - 128KB ROM
  - 4Kb eFuse
  - 内嵌 2/4/8MB Flash (选配)
  - 内嵌 4/8MB pSRAM (选配，仅在 BL618 支持)
- Video/Image(仅在 BL618 支持)
  - Camera Sensor DVP 接口
  - LCD 显示 (QSPI, DBI 和 RGB)
  - Video Codec MJPEG encoding
- 安全
  - 安全启动; 安全调试
  - XIP On-The-Fly AES 解密 (OTFAD)
  - 支持 TrustZone
  - AES-CBC/CCM/GCM/XTS 模式
  - MD5、SHA-1/224/256/384/512
  - TRNG（真随机数生成器）
  - 用于 RSA/ECC 的 PKA（公钥加速器）
- 外设

[1]532K SRAM 包含 4K HBN RAM，16K Dcache RAM 和 32K Icache RAM。

  - USB 2.0 HS OTG (High-Speed 480MHz)
  - SDIO 2.0 从机
  - SD 卡接口
  - 2 个 UART（支持 5V IO）
  - 2 个 I2C，支持主机模式
  - SPI 主/从
  - I2S 主/从
  - 1 个 PWM 控制器（带互补输出的 4 通道）
  - 12-bit~16-bit 通用 ADC
  - 12-bit 通用 DAC
  - 通用模拟比较器 (ACOMP)
  - 可配置的 19 (BL616) 或 35 (BL618) 个 GPIO

- 功耗模式（超低功耗模式）
  - 关闭; 休眠 (<1uA)
  - 掉电睡眠（灵活）
- 时钟
  - 支持 XTAL 24/26/32/38.4/40MHz
  - 支持 XTAL 32.768KHz
  - 内部 RC 32KHz /32MHz 振荡器
  - 内部 System /Audio PLL
- 封装类型
  - 40 pin QFN (BL616)
  - 56 pin QFN (BL618)

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1 概述

BL616/BL618 是一款适用于超低功耗应用的 Wi-Fi 6 + 蓝牙 5.3 + 802.15.4(Zigbee/Thread) 组合芯片。主要包含无线和微控制器两个子系统。

无线子系统包含 2.4G 无线电、Wi-Fi 802.11b/g/n/ax、BT/BLE 和 802.15.4 基带/MAC 设计。

微控制器子系统包含一个带有浮点单元、DSP 单元、高速缓存和存储器的低功耗 32 位 RISC-V CPU，最高主频可达 320M。

此外，芯片具有丰富的外设接口，具体包括 Camera(仅在 BL618 支持)、Dispaly(仅在 BL618 支持)、MJPEG(仅在 BL618 支持)、Audio Codec(仅在 BL618 支持)、USB2.0、SDU、以太网 (EMAC, 仅在 BL618 支持)、SD/MMC(SDH)、SPI、UART、I2C、I2S、PWM、GPDAC、GPADC、ACOMP 等，可以应用于音视频等多媒体领域和工业领域。

BL616/BL618 电源管理单元控制低功耗模式，支持 PDS(Power Down Sleep) 和 HBN(Hibernate) 两种低功耗模式，支持多种唤醒源以满足不同的低功耗场景。Sec Eng 模块支持 AES/SHA/PKA/TRNG 等功能，支持镜像加密和签名启动，满足物联网领域的各种安全应用需求。BL616 共有 19 个 GPIO，BL618 共有 35 个 GPIO，其系统功能框图如下所示。

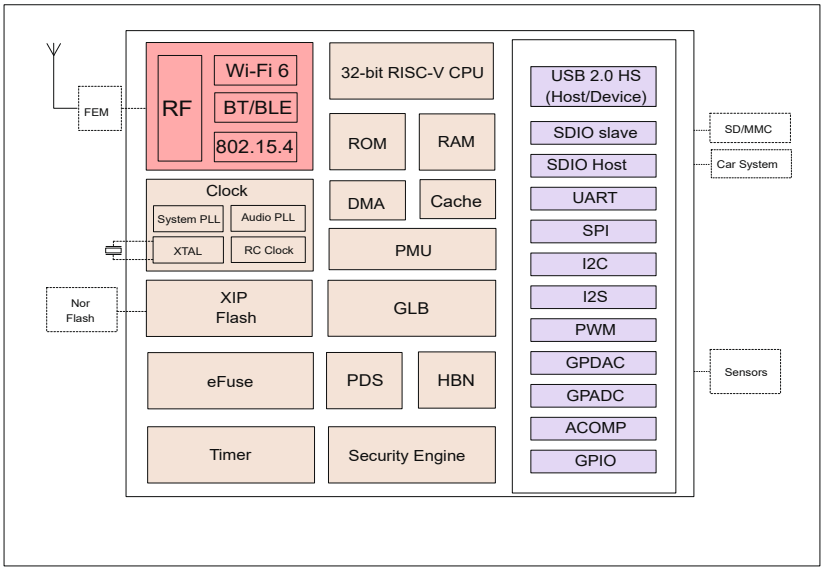

图 1.1: BL616 功能框图

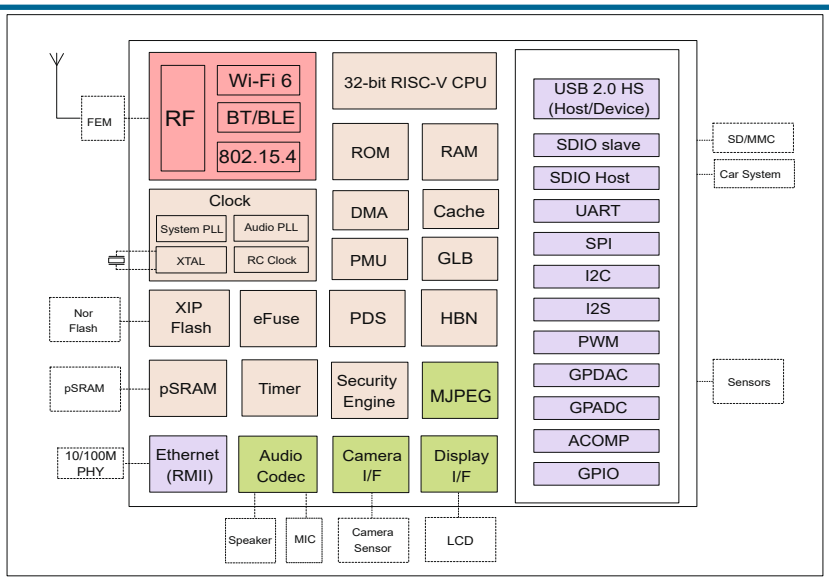

图 1.2: BL618 功能框图

表 1.1: BL61x 特性和外设个数

对比项	BL616	BL618
CPU	E907@ 320MHz	E907@ 320MHz
I-Cache	32K	32K
D-Cache	16K	16K
SRAM	484K	484K
PSRAM	X	4M
eFuse	4K	4K
ROM	128K	128K
Flash	内封/外置，容量根据型号确定	一般外置，容量根据型号确定
UART	2 路	2 路
SPI	1 路	1 路
EMAC	X	✓
USB 2.0	✓	✓
SDIO slave	✓	✓
SDIO Host	✓	✓
I2C	2 路	2 路
I2S	1 路	1 路
PWM	1 路 (带互补输出的 4 通道)	1 路（带互补输出的 4 通道)
GPADC	11 通道	12 通道
GPDAC	✓(GPIO2/3)	✓(GPIO2/3)
ACOMP	✓	✓
GPIO	19	35

表 1.1: BL61x 特性和外设个数 (continued)

对比项	BL616	BL618
DMA	✓	✓
GLB	✓	✓
PDS	✓	✓
HBN	✓	✓
MJPEG	X	✓
SEC ENG	✓	✓
Display	X	✓
CAM	X	✓
Audio DAC	X	✓
Audio ADC	X	✓
Timer	✓	✓
IR(RX)	✓(GPIO10-17,GPIO20-22)	✓(GPIO9-23)

2 功能描述

BL616/BL618 系统架构如下所示:

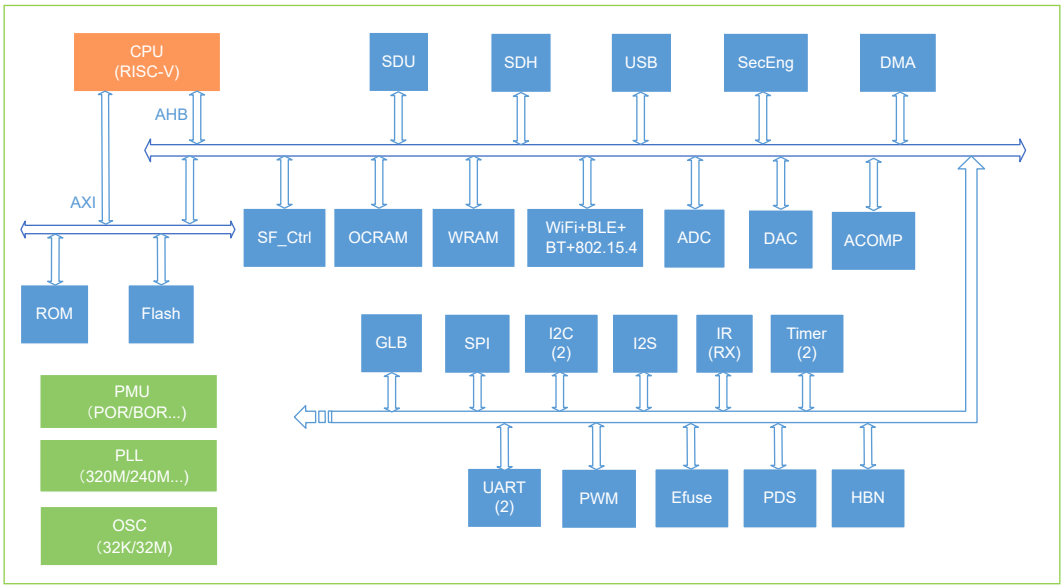

图 2.1: BL616 系统架构图

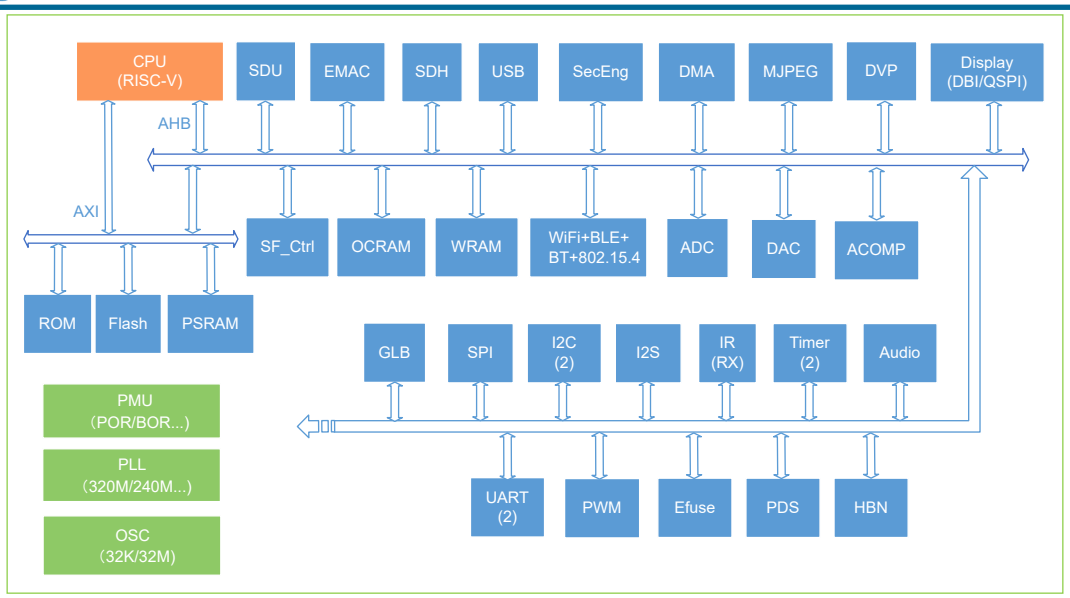

图 2.2: BL618 系统架构图

CPU 带有 AXI 和 AHB 两条总线，ROM，Flash 和 PSRAM(仅在 BL618 支持) 挂在 AXI 总线上，以实现对这些存储单元的高速访问，各个外设通过 AHB 总线与 CPU 连接在一起。

2.1 CPU

BL616/BL618 内置一颗 32-bit RISC-V CPU，它采用 5 级流水线结构：取指、译码、执行、内存访问、写回，支持 RISC-V 32/16 位混编指令集，包含 64 个外部中断源，有 4 个 bits 可以用于配置中断优先级。

2.2 缓存

BL616/BL618 的缓存提高了 CPU 访问外部存储器的效能，包含 32K 指令 cache 和 16K 数据 cache。

2.3 内存

BL616/BL618 存储器包括：片上零延迟 SRAM 存储器，只读存储器，一次写入存储器，嵌入式闪存（可选），嵌入式 pSRAM（可选，仅在 BL618 支持）。

2.4 DMA 控制器

BL616/BL618 DMA（直接存储器访问）控制器具有 4 个专用通道，用于管理外设和存储器之间的数据传输，以提高 CPU /总线效率。DMA 有四种传输类型，内存到内存，内存到外设、外设到内存以及外设到外设四种模式。

DMA 还支持 LLI（链接列表项）功能，该链表由一系列链接列表预定义多个传输，然后硬件会根据每个 LLI 的大小和地址自动完成所有传输。

DMA 支持的外设包括 UART、I2C、SPI、Audio(Audio ADC 和 Audio DAC, 仅在 BL618 支持)、GPIO、I2S、DBI（仅在 BL618 支持）、GPADC、GPDAC。

2.5 地址映射

表 2.1: 内存地址映射

模块	大小	开始地址	
		Cache	Non-cache
OCRAM	320KB	0x62FC0000	0x22FC0000
WRAM	160KB	0x63010000	0x23010000

OCRAM 和 WRAM 既可以通过 AHB 总线访问，也可以通过 AXI 访问，当 CPU 使用 0x62FC0000 地址访问 OCRAM 时，会经过内部 Cache 并通过 AXI 转 AHB 实现对 OCRAM 的访问，当 CPU 使用 0x22FC0000 地址访问 OCRAM 时，不会经过内部 Cache 并且直接通过 AHB 总线访问 OCRAM 。

表 2.2: 地址映射

模块	目标	开始地址	大小	描述
FLASH	Flash	0xA0000000	128MB	应用程序地址空间
PSRAM	pSRAM	0xA8000000	128MB	pSRAM 存储器地址空间 (可选项，依赖芯片具体型号，仅在 BL618 支持)
RAM	HBN RAM	0x20010000	4KB	HBN RAM, 主要用于超低功耗模式下的数据保存
Peripheral	USB	0x20072000	4KB	USB High Speed OTG 控制寄存器
	EMAC	0x20070000	4KB	EMAC 控制寄存器（仅在 BL618 支持）
	SDH	0x20060000	4KB	SDH 控制寄存器
	MJPEG	0x20059000	4KB	MJPEG 图像编码控制寄存器（仅在 BL618 支持）
	DVP	0x20057000	4KB	DVP 摄像头接口控制寄存器（仅在 BL618 支持）
	Efuse	0x20056000	4KB	Efuse 存储控制寄存器
	AUDIO DAC	0x20055000	4KB	Audio DAC 控制寄存器（仅在 BL618 支持）
	PSRAM_Ctrl	0x20052000	4KB	PSRAM 控制寄存器（仅在 BL618 支持）
	HBN	0x2000F000	4KB	深度睡眠控制（休眠）寄存器
	PDS	0x2000E000	4KB	睡眠控制（掉电睡眠）寄存器
	SDU	0x2000D000	4KB	SDU 控制寄存器
	DMA	0x2000C000	4KB	DMA 控制寄存器
	SF_Ctrl	0x2000B000	4KB	Serial Flash 控制寄存器
	Audio ADC	0x2000AC00	256B	Audio ADC 控制寄存器（仅在 BL618 支持）
	I2S	0x2000AB00	256B	I2S 控制寄存器
	I2C1	0x2000A900	256B	I2C1 控制寄存器
	Display	0x2000A800	256B	Display 控制寄存器（仅在 BL618 支持）
	IRR	0x2000A600	256B	IR Receiver 控制寄存器
	TIMER	0x2000A500	256B	TIMER 控制寄存器

表 2.2: 地址映射 (continued)

模块	目标	开始地址	大小	描述
	PWM	0x2000A400	256B	PWM 控制寄存器
	I2C0	0x2000A300	256B	I2C0 控制寄存器
	SPI	0x2000A200	256B	SPI 控制寄存器
	UART1	0x2000A100	256B	UART1 控制寄存器
	UART0	0x2000A000	256B	UART0 控制寄存器
	TZ	0x20005000	4KB	TrustZone 控制寄存器
	SEC_ENG	0x20004000	4KB	安全引擎控制寄存器
	GPIP	0x20002000	1KB	通用 DAC/ADC/ACOMP 接口控制寄存器
	GLB	0x20000000	4KB	全局控制寄存器
ROM	ROM	0x90000000	128KB	Bootrom 区域地址空间

2.6 中断

BL616/BL618 中断控制器支持 UART/I2C/SPI/Timer/DMA/EMAC（仅在 BL618 支持）/WiFi/BLE 等共 64 个可屏蔽中断触发源。

所有 I/O 引脚都可以配置为外部中断输入模式，外部中断支持同步高/低电平触发、同步上升沿/下降沿触发、异步高/低电平触发、异步上升沿/下降沿触发和同步双边沿触发共 9 种触发类型。

2.7 启动选项

BL616/BL618 支持多种启动选项，可选择从 Flash/UART/USB/SDU 启动。

表 2.3: 启动模式

启动引脚	电平	描述
GPIO2	1	从 UART(GPIO21/22)/USB/SDU 启动，该模式主要用于 Flash 烧写或者下载镜像到 RAM 执行 (无线透传场景)
	0	从 Flash 启动应用镜像

2.8 电源管理单元

电源管理单元（PMU）管理整个芯片的电源，芯片中有 8 个电源域：PD_AON/PD_AON_HBNRTC/PD_AON_HBNCORE/PD_CORE/PD_CORE_MISC/PD_USB/PD_CPU/PD_WB。可以实现的低功耗模式包括运行、空闲、睡眠 (PDS)、休眠 (HBN) 和电源关闭。在睡眠 (PDS) 和休眠 (HBN) 模式下，可以有多种唤醒源将系统从低功耗模式唤醒。

2.9 时钟架构

时钟控制单元为核心 MCU 和外围 SOC 设备生成时钟。时钟源可以是 XTAL，PLL 或 RC 振荡器。用户可以通过适当的配置（例如 sel，div，en 等）来设定各个外设的时钟频率或者开关外设的时钟，以达到低功耗的应用需求。

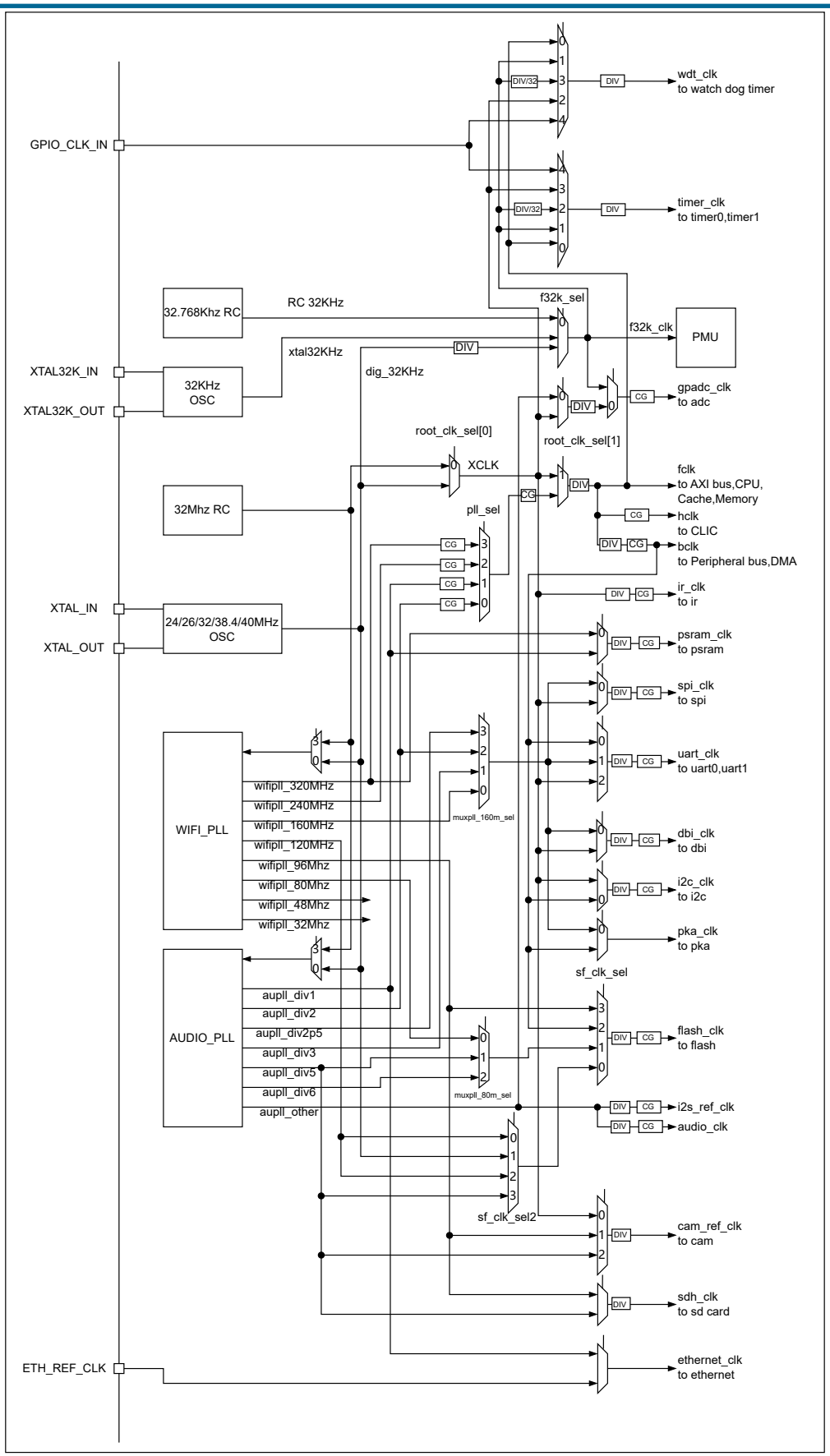
GPIO_CLK_IN
32.768Khz RC
RC 32KHz
XTAL32K_IN
XTAL32K_OUT
32KHz OSC
xtal32KHz
dig_32KHz
32Mhz RC
XTAL_IN
XTAL_OUT
24/26/32/38.4/40MHz OSC
WIFI_PLL
wifipll_320MHz
wifipll_240MHz
wifipll_160MHz
wifipll_120MHz
wifipll_96Mhz
wifipll_80Mhz
wifipll_48Mhz
wifipll_32Mhz
AUDIO_PLL
aupll_div1
aupll_div2
aupll_div2p5
aupll_div3
aupll_div5
aupll_div6
aupll_other
ETH_REF_CLK
DIV/32
DIV
wdt_clk
to watch dog timer
timer_clk
to timer0,timer1
f32k_sel
f32k_clk
PMU
CG
gpadc_clk
to adc
root_clk_sel[0]
root_clk_sel[1]
XCLK
fclk
to AXI bus,CPU,
Cache,Memory
hclk
to CLIC
bclk
to Peripheral bus,DMA
pll_sel
ir_clk
to ir
psram_clk
to psram
spi_clk
to spi
uart_clk
to uart0,uart1
dbi_clk
to dbi
i2c_clk
to i2c
pka_clk
to pka
sf_clk_sel
flash_clk
to flash
muxpll_160m_sel
muxpll_80m_sel
i2s_ref_clk
audio_clk
sf_clk_sel2
cam_ref_clk
to cam
sdh_clk
to sd card
ethernet_clk
to ethernet

图 2.3: 时钟框图

2.10 外设

外设包括 GPIO，UART，SPI，I2C，PWM，Timer，IR(RX)，I2S，Audio(Audio ADC+Audio DAC, 仅在 BL618 支持)，SDU，MJPEG（仅在 BL618 支持），SD/MMC(SDH)，Ethernet MAC（仅在 BL618 支持），GPDAC，GPADC，ACOMP，USB2.0。

2.10.1 GPIO

BL616 最多可达 19 个 GPIO，BL618 最多可达 35 个 GPIO，具有以下特性：

- 每个 GPIO 都可用作通用输入和输出功能，上拉/下拉/浮空可由软件配置
- 每个 GPIO 都支持中断功能，中断支持同步高/低电平触发、同步上升沿/下降沿触发、异步高/低电平触发、异步上升沿/下降沿触发和同步双边沿触发
- 每个 GPIO 均可设置为高阻态，用于低功耗模式
- 每个 GPIO 均可通过 Set/Clear 寄存器完成输出状态的控制
- 支持自定义的逻辑 0/1 波形输出
- 支持 DMA

2.10.2 UART

芯片内置两个通用异步串行收发器 (UART0/1)，具有以下特性：

- 支持硬件的 CTS 和 RTS 流控
- 支持 LIN 主/从功能
- 可配置的数据位、停止位和奇偶校验位
- 支持普通/固定字符的自动波特率检测
- 工作时钟可以选择为 FCLK 、XCLK 或 160MHz，波特率最大支持 10Mbps
- TX 和 RX 具有独立 FIFO，FIFO 深度为 32 字节，支持 DMA 功能

2.10.3 SPI

芯片内置一个 SPI，可以配置为主机模式或者从机模式，SPI 模块时钟是 XCLK 或 160MHz，具有以下特性：

- 主机模式下，时钟频率最高为 80 MHz
- 从机模式下，允许主机最大的时钟频率为 80 MHz
- 每帧的位宽可以配置为 8 位/ 16 位/ 24 位/ 32 位
- 自适应的 FIFO 深度变化特性，适配高性能的场景应用

  - 当位宽为 32 位时，FIFO 的深度为 8
  - 当位宽为 24 位时，FIFO 的深度为 8
  - 当位宽为 16 位时，FIFO 的深度为 16
  - 当位宽为 8 位时，FIFO 的深度为 32
- 支持 DMA 传输模式

2.10.4 I2C

芯片内置两个 I2C 接口，具有以下特性：

- 支持多主机模式和仲裁功能
- 工作时钟可以选择为 BCLK 或者 XCLK
- 具有器件地址寄存器，寄存器地址寄存器，寄存器地址长度可设置为 1 字节/ 2 字节/ 3 字节/ 4 字节
- I2C 具有独立收发 FIFO，FIFO 深度为 2 word
- 支持 DMA 功能

2.10.5 EMAC（仅在 BL618 支持）

EMAC 模块是一个兼容 IEEE 802.3 的 100Mbps 以太网 MAC(Ethernet Media Access Controller)，具有以下特性：

- 兼容 IEEE 802.3 定义的 MAC 层功能
- 支持 IEEE 802.3 定义的 MII/RMII 接口的 PHY
- 通过 MDIO 接口与 PHY 交互
- 支持 100Mbps 以太网
- 支持半双工与全双工
- 在全双工模式下，支持自动流控及生成控制帧
- 在半双工模式下，支持碰撞检测及重传
- 支持 CRC 的生成及校验
- 数据帧前导生成及移除
- 发送时，自动扩展短的数据帧
- 检测过长或过短的数据帧 (长度限制)
- 可传输长数据帧 (> 标准以太帧长度)
- 自动丢弃重发次数超限或帧间隙过小的数据包

- 广播包过滤
- 用于保存多达 128 个 BD(Buffer Descriptor) 的内部 RAM
- 在发送时，支持将一个数据包分拆配置到多个连续的 BD
- 发送/接收的各种事件标志
- 在事件发生时产生对应中断

EMAC 时序图如下所示：

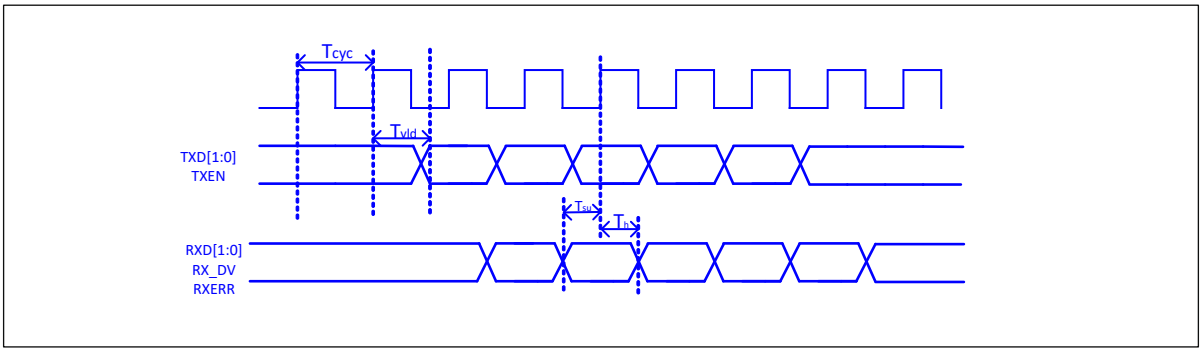

图 2.4: EMAC 时序图

表 2.4: 使用 RX Clock 对应的时序条件

将寄存器 eth_cfg0 对应的位设置为：cfg_inv_eth_rx_clk = 1，cfg_inv_eth_tx_clk = 0，cfg_sel_eth_ref_clk_o = 0						
时序参数（1.8V, Load = 20PF）		最小值	典型值	最大值	单位	备注
T_{cyc}	Clock Cycle	-	20	-	ns	Clock From ETH PHY
T_{vld}	Output Valid Delay	6.98	-	15.63	ns	TXD/TX_EN
T_{su}	Input Setup Time	11.64	-	-	ns	RXD/RX_DV/RXERR
T_h	Input Hold Time	0	-	-	ns	RXD/RX_DV/RXERR

表 2.5: 不使用 RX Clock 对应的时序条件

将寄存器 eth_cfg0 对应的位设置为：cfg_inv_eth_rx_clk = 0，cfg_inv_eth_tx_clk = 0，cfg_sel_eth_ref_clk_o = 0						
时序参数（1.8V, Load = 20PF）		最小值	典型值	最大值	单位	备注
T_{cyc}	Clock Cycle	-	20	-	ns	Clock From ETH PHY
T_{vld}	Output Valid Delay	6.98	-	15.63	ns	TXD/TX_EN
T_{su}	Input Setup Time	3.5	-	-	ns	RXD/RX_DV/RXERR
T_h	Input Hold Time	2	-	-	ns	RXD/RX_DV/RXERR

2.10.6 I2S

芯片内置一个 I2S 接口，具有以下特性：

- 支持主模式以及从模式
- 支持 Left-justified/ Right-justified/ DSP 等数据格式，数据宽度可配置为 8/16/24/32 比特
- 工作时钟为 Audio PLL
- 除单声道/双声道模式之外，同时支持四声道与六声道模式
- 支持播放单声道音频复制为双声道模式
- 支持动态静音切换功能
- I2S 具有独立收发 FIFO，FIFO 深度为 16 word
- 支持 DMA 功能

2.10.7 TIMER

芯片内置两个 32-bit 通用定时器和一个看门狗定时器，具有以下特性：

- 通用定时器的时钟源可以选择 FCLK/32K/XTAL，看门狗定时器的时钟源可以选择 FCLK/32K/XTAL
- 每个计数器都有 8-bit 分频器
- 每组通用定时器都包含三个比较寄存器，支持比较中断，计数模式支持 FreeRun 模式和 PreLoad 模式
- 16-bit 看门狗定时器，支持中断或复位两种看门狗溢出方式

2.10.8 PWM

芯片内置一组 PWM 信号，每组包含 4 通道 PWM 信号输出，每通道可以设置为 2 路互补 PWM，具有以下特性：

- 三种时钟源 BCLK/XCLK/32K 可供选择，搭配 16-bit 时钟分频器
- 每组 PWM 都可以独立设置为不同的周期
- 每通道 PWM 都有双门限值设定，可以设定不同的占空比和相位，增加脉冲弹性
- 每通道 PWM 都有独立的死区时间设定
- 每路 PWM 输出引脚都可以设定不同的有效电平
- 每路 PWM 都有独立的连接开关用来选择是否与内部计数器相连，并可设定不连接时的默认输出电平
- 刹车信号可以将 PWM 输出电平置于预先设定的状态
- 多达 11 种可用于触发 ADC 转换的触发源
- 支持多种中断类型：计数器溢出中断、门限值比较中断、周期数中断

2.10.9 IR(IR-remote)

芯片内置一个红外遥控，具有以下特性：

- 既支持以固定协议 NEC、RC-5 接收数据，也支持以脉冲宽度计数方式接收任意格式数据
- 时钟源为 XCLK，最高工作频率为 40MHz
- 接收最多支持 64-bit 数据位
- 接收 FIFO 深度为 128 字节
- 支持接收结束中断

2.10.10 Audio ADC（仅在 BL618 支持）

- 集成 1 路音频 ADC（与高精度 ADC 不可同时使用），具有以下特性：
  - 采样率:8k~96k
  - 信噪比 (A-W)：96dB@6dB 增益，48K 采样率
  - 谐波失真 + 噪声：-90dB@6dB 增益，48K 采样率
  - 模拟前置增益：6~42 dB, 3dB 一档
  - 模拟全差分输入或单端输入
- 可调节的高通滤波器和数字音量控制
- 支持 PDM 接口（支持 1 路 DMIC）
- 输入信号复用 GPIO
- 32 位宽度的发送 FIFO，深度为 8
- 支持 DMA 传输模式

2.10.11 Audio DAC（仅在 BL618 支持）

- 集成 1 路音频 DAC，具有以下特性：
  - 采样率:8k~48k
  - 信噪比 (A-W)：95dB@48K 采样率
  - 谐波失真 + 噪声：-80dB@48K 采样率
- 可调节的数字音量控制
- 支持差分互补输出
- 输出信号复用 GPIO

- 32 位宽度的发送 FIFO，深度为 16
- 支持 DMA 传输模式

2.10.12 GPADC

芯片内置一个 12bits 的逐次逼近式模拟数字转换器 (ADC)，具有以下特性：

- 单通道连续转换模式最高采样率可达 2M，其它转换模式最高采样率 500K
- 支持 12 路外部模拟通道
- 支持单通道单次转换、单通道连续转换、多通道单次转换、多通道连续转换
- 支持 2.0V，3.2V 可选内部参考电压，转换结果为 12/14/16bits(通过过采样实现) 左对齐模式
- 拥有深度为 32 字节的 FIFO，支持多种中断，支持 DMA 功能
- ADC 除了用于普通模拟信号测量外，还可以用于测量供电电压
- 可以通过测量内/外部二极管电压用于温度检测

2.10.13 高精度 ADC

- 芯片内置 1 路高精度 ADC（与 audio CODEC 不可同时使用），具有以下特性：
  - 支持全差分输入，4 通道
  - 有效分辨率 (ER)：19.5bit
  - 可编程增益放大器：6dB~42dB（2 至 128 倍），3dB 一档
  - 可编程数据传输率：20SPS、100SPS、200SPS、400SPS、1000SPS、2000SPS
  - 支持高精度/低延迟双套数字滤波器
  - 支持 50Hz/60Hz 同步工频抑制
  - 支持软件全局斩波，ER=20.7bit，低于 1uV 的失调电压
- 复用 GPIO 输入信号
- 32 位宽度的发送 FIFO，深度为 8
- 支持轮询、中断、DMA 传输模式

2.10.14 SDIO

SDIO 时序图如下所示：

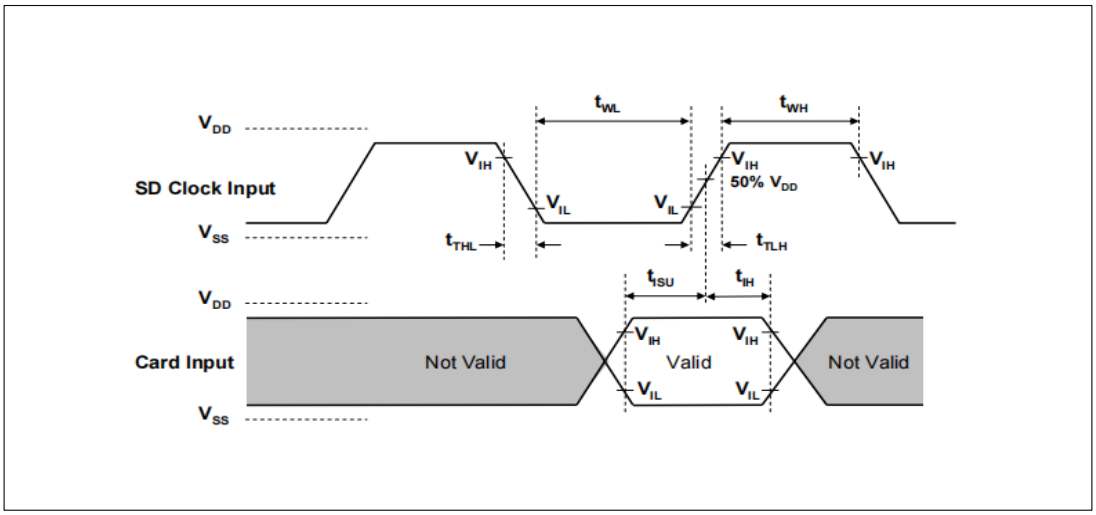

图 2.5: Card 输入时序图

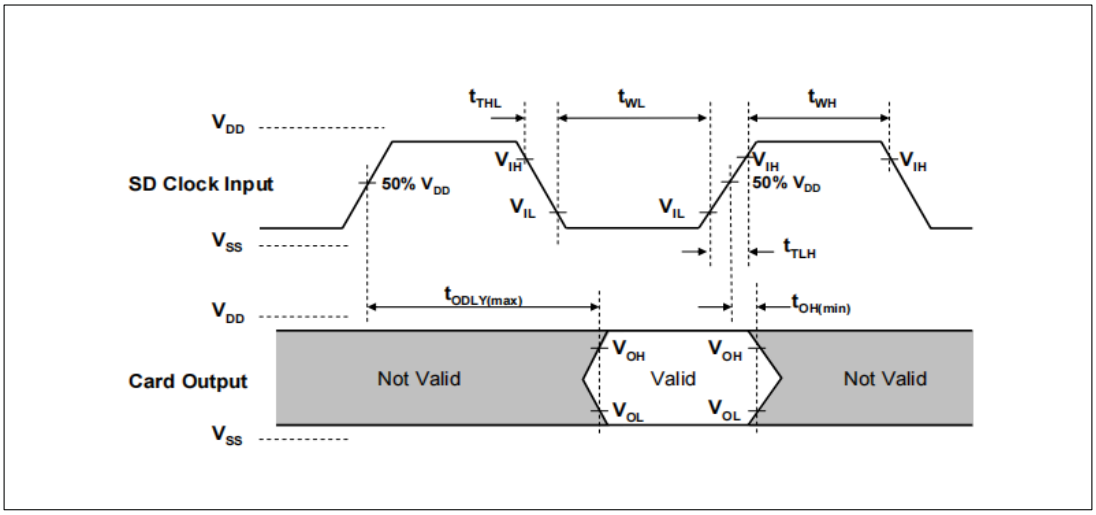

图 2.6: Card 输出时序图

表 2.6: 时序图参数说明

符号	参数	条件	最小值	典型值	最大值	单位
Clock CLK (All values are referred to min (VIH) and max (VIL))						
f_{PP}	Clock frequency Data Transfer Mode	C_{CARD}≤ 10 pF (1 card)	0		50	MHz
t_{WL}	Clock low time	C_{CARD}≤ 10 pF (1 card)	7			ns
t_{WH}	Clock high time	C_{CARD}≤ 10 pF (1 card)	7			ns

表 2.6: 时序图参数说明 (continued)

符号	参数	条件	最小值	典型值	最大值	单位
t_{TLH}	Clock rise time	C_{CARD}≤ 10 pF (1 card)			3	ns
t_{THL}	Clock fall time	C_{CARD}≤ 10 pF (1 card)			3	ns
Inputs CMD, DAT (referenced to CLK)						
t_{ISU}	Input set-up time	C_{CARD}≤ 10 pF (1 card)	6			ns
t_{IH}	Input hold time	C_{CARD}≤ 10 pF (1 card)	2			ns
Outputs CMD, DAT (referenced to CLK)						
t_{ODLY}	Output Delay time during Data Transfer Mode	C_L≤ 40 pF (1 card)			14	ns
t_{OH}	Output Hold time	C_L≥ 15 pF (1 card)	2.5			ns
C_L	Total System capacitance for each line [1]	1 card			40	pF

[1] In order to satisfy stringent timing, host shall drive only one card.

3 管脚定义

BL616 40-pin 封装包括固定电源接口 15 个、固定模拟接口 6 个、可配置的 GPIO 接口最多可达 19 个。

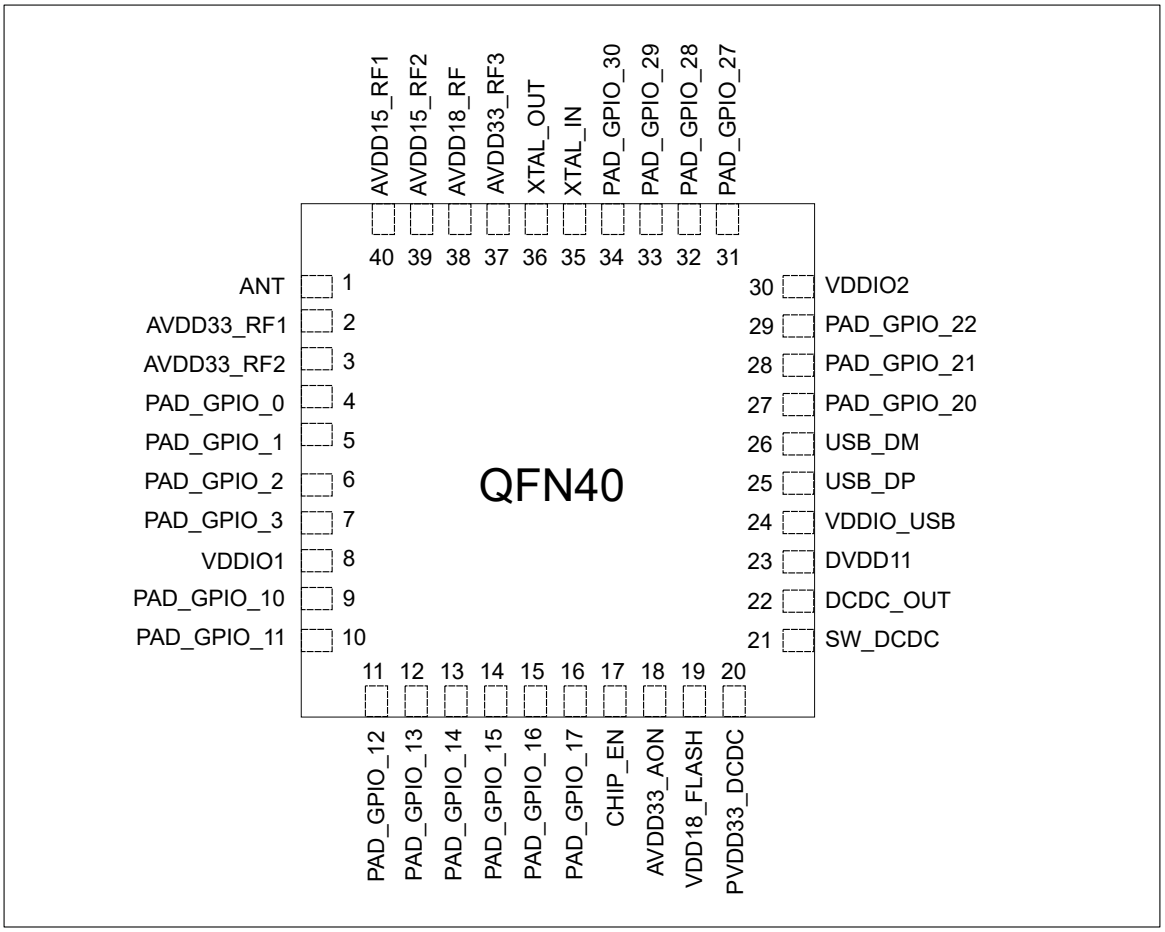

图 3.1: BL616 管脚布局

BL618 56-pin 封装包括固定电源接口 15 个、固定模拟接口 6 个、可配置的 GPIO 接口最多可达 35 个。

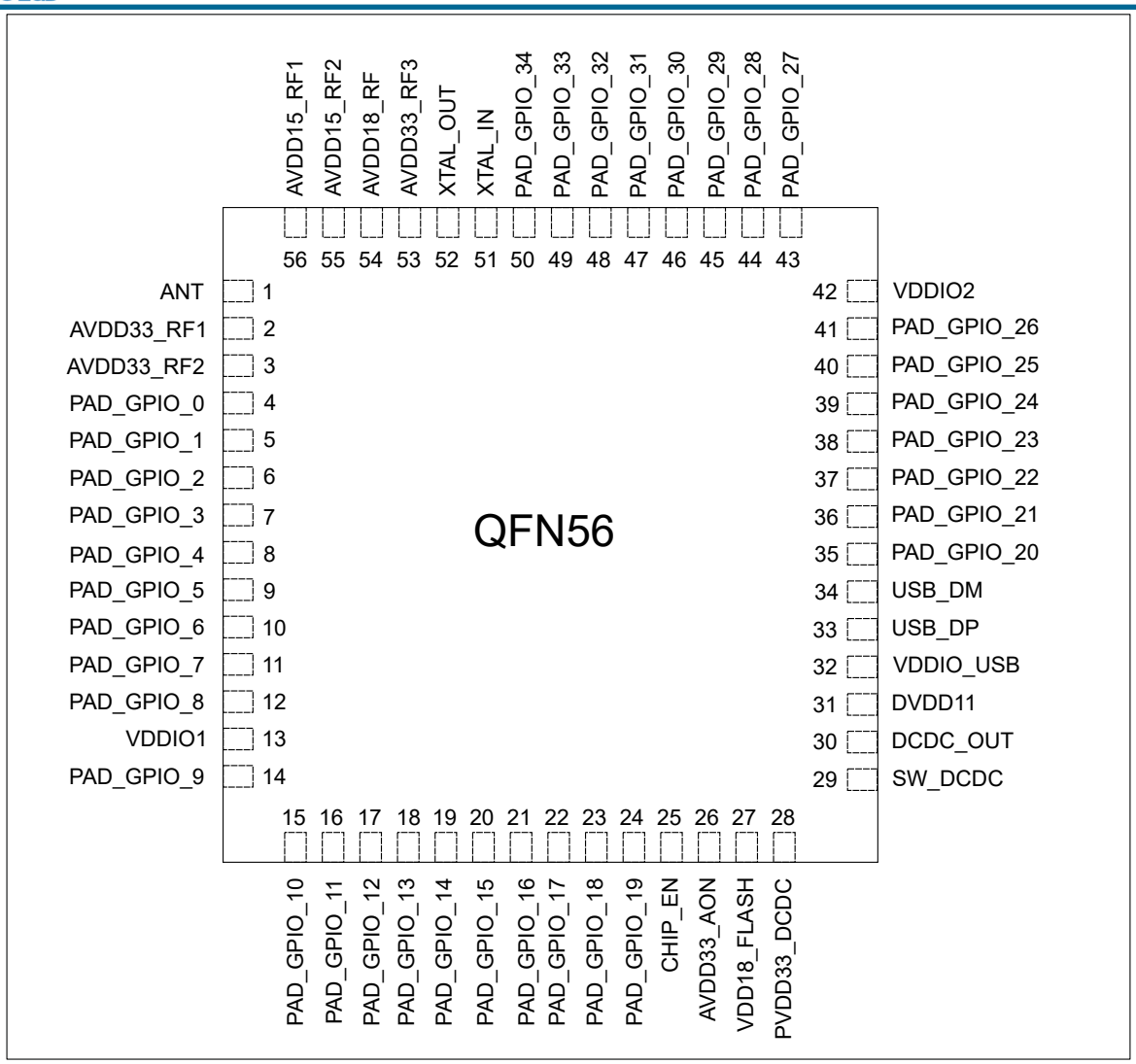

图 3.2: BL618 管脚布局

表 3.1: 管脚定义

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
1	1	AVDD15_RF1	Analog	ANT	-	-	ANT	RF signal pin
2	2	-	Power,Input	AVDD33_RF1	-	-	AVDD33_RF1	RF transmitter power supply, 3.3V
3	3	-	Power,Input	AVDD33_RF2	-	-	AVDD33_RF2	RF transmitter power supply, 3.3V

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
4	4	VDDIO_1	DI/DO	PAD_GPIO_0	0	-	-	-
					1	-	SPI_SS	SPI Slave Select
					2	-	-	-
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_0_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_0_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_0_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_0_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_0_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_0_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_0_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_0_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	CAM1_VSYNC [1]	Camera 1 Vertical Sync (Only for BL618)
					10	-	ADC_CH9	ADC Channel 9
					11	-	SWGPIO0	Software GPIO 0
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0 Channel 0 Positive
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
5	5	VDDIO_1	DI/DO	PAD_GPIO_1	0	-	-	-
					1	-	SPI_SCLK	SPI Serial Clock
					2	-	-	-
					3	-	I2S_FS	I2S Frame Sync
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_1_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_1_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_1_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_1_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_1_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_1_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_1_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_1_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	CAM1_HSYNC	Camera 1 Horizontal Sync (Only for BL618)
					10	-	ADC_CH8	ADC Channel 8
					11	-	SWGPIO1	Software GPIO1
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0 Channel 0 Negative
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TCK	M0 JTAG Test Clock

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
6	6	VDDIO_1	DI/DO	PAD_GPIO_2	0	-	-	
					1	-	SPI_MISO [2]	SPI Master Input, Slave Output
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_2_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_2_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_2_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_2_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_2_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_2_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_2_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_2_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH2	ADC Channel 2
					11	-	SWGPIO2	Software GPIO 2
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0 Channel 1 Positive
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDO	M0 JTAG Test Data Out

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
7	7	VDDIO_1	DI/DO	PAD_GPIO_3	0	-	-	-
					1	-	SPI_MOSI	SPI Master Output, Slave Input
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_3_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_3_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_3_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_3_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_3_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_3_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_3_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_3_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	CAM1_DAT0	Camera 1 Data 0 (Only for BL618)
					10	-	ADC_CH3	ADC Channel 3
					11	-	SWGPIO3	Software GPIO 3
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0 Channel 1 Negative
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDI	M0 JTAG Test Data Input

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	8	VDDIO_1	DI/DO	PAD_GPIO_4	0	-	-	-
					1	-	SPI_SS	SPI Slave Select
					2	-	SF2_CS [3]	NOR FALSH controller signal2 Chip Select
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_4_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_4_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_4_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_4_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_4_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_4_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_4_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_4_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO4	Software GPIO 4
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0 Channel 2 Positive
					22	-	DBI_TypeB_WRn	Display Bus Interface Type B Write Control (Only for BL618)
					23	-	DBI_TypeC_SCL	Display Bus Interface Type C Serial Clock (Only for BL618)
					24	-	DISP_QSPI_SCL	Display Quad SPI Serial Clock (Only for BL618)
					25	-	-	-
					26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	9	VDDIO_1	DI/DO	PAD_GPIO_5	0	-	-	-
					1	-	SPI_SCLK	SPI Serial Clock
					2	-	SF2_D1	NOR FALSH controller signal2 Data 1
					3	-	I2S_FS	I2S Frame Sync
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_5_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_5_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_5_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_5_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_5_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_5_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_5_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_5_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO5	Software GPIO 5
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0 Channel 2 Negative
					22	-	DBI_TypeB_CSn	Display Bus Interface Type B Chip Select (Only for BL618)
					23	-	DBI_TypeC_CSn	Display Bus Interface Type C Chip Select (Only for BL618)
					24	-	DISP_QSPI_CSn	Display Quad SPI Chip Select (Only for BL618)
					25	-	-	-
					26	-	M0_JTAG_TCK	M0 JTAG Test Clock

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	10	VDDIO_1	DI/DO	PAD_GPIO_6	0	-	-	-
					1	-	SPI_MISO	SPI Master Input, Slave Output
					2	-	SF2_D2	NOR FALSH controller signal2 Data 2
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_6_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_6_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_6_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_6_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_6_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_6_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_6_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_6_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO6	Software GPIO 6
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0 Channel 3 Positive
					22	-	DBI_TypeB_RDn	Display Bus Interface Type B Read Control (Only for BL618)
					23	-	DBI_TypeC_SDA0	Display Bus Interface Type C Serial Data 0 (Only for BL618)
					24	-	DISP_QSPI_SDA0	Display Quad SPI Serial Data 0 (Only for BL618)
					25	-	-	
					26	-	M0_JTAG_TDO	M0 JTAG Test Data Out

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	11	VDDIO_1	DI/DO	PAD_GPIO_7	0	-	-	-
					1	-	SPI_MOSI	SPI Master Output, Slave Input
					2	-	SF2_D0	NOR FALSH controller signal2 Data 0
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_7_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_7_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_7_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_7_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_7_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_7_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_7_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_7_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO7	Software GPIO 7
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0 Channel 3 Negative
					22	-	DBI_TypeB_DCn	Display Bus Interface Type B Data /Command Control (Only for BL618)
					23	-	DBI_TypeC_DCn	Display Bus Interface Type C Data /Command Control (Only for BL618)
					24	-	DISP_QSPI_SDA1	Display Quad SPI Serial Data 1 (Only for BL618)
					25	-	-	-
					26	-	M0_JTAG_TDI	M0 JTAG Test Data Input

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	12	VDDIO_1	DI/DO	PAD_GPIO_8	0	-	-	-
					1	-	SPI_SS	SPI Slave Select
					2	-	SF2_CLK	NOR FALSH controller signal2 Clock
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_8_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_8_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_8_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_8_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_8_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_8_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_8_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_8_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO8	Software GPIO 8
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0 Channel 0 Positive
					22	-	DBI_TypeB_DB0	Display Bus Interface Type B Data Bit 0 (Only for BL618)
					23	-	DBI_TypeC_SCL	Display Bus Interface Type C Serial Clock (Only for BL618)
					24	-	DISP_QSPI_SDA2	Display Quad SPI Serial Data 2 (Only for BL618)
					25	-	-	-
					26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select
8	13	-	Power,Input	VDDIO1	-	-	VDDIO1	1.8V/3.3V power supply of GPIO0 - GPIO19

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	14	VDDIO_1	DI/DO	PAD_GPIO_9	0	-	-	-
					1	-	SPI_SCLK	SPI Serial Clock
					2	-	SF2_D3	NOR FALSH controller signal2 Data 3
					3	-	I2S_FS	I2S Frame Sync
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_9_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_9_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_9_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_9_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_9_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_9_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_9_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_9_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO9	Software GPIO 9
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0 Channel 0 Negative
					22	-	DBI_TypeB_DB1	Display Bus Interface Type B Data Bit 1 (Only for BL618)
					23	-	DBI_TypeC_CSn	Display Bus Interface Type C Chip Select (Only for BL618)
					24	-	DISP_QSPI_SDA3	Display Quad SPI Serial Data 3 (Only for BL618)
					25	-	-	-
					26	-	M0_JTAG_TCK	M0 JTAG Test Clock

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
9	15	VDDIO_1	DI/DO	PAD_GPIO_10	0	-	SDH_DAT1	SD Host Data 1
					1	-	SPI_MISO	SPI Master Input, Slave Output
					2	-	SF3_D3	NOR FALSH controller signal3 Data 3
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_10_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_10_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_10_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_10_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_10_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_10_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_10_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_10_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	CAM1_DAT1	Camera 1 Data 1 (Only for BL618)
					10	-	ADC_CH7	ADC Channel 7
					11	-	SWGPIO10	Software GPIO 10
					12	-	SDIO_DAT2	SDIO Data 2
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0 Channel 1 Positive
					22	-	DBI_TypeB_DB2	Display Bus Interface Type B Data Bit 2 (Only for BL618)
					23	-	DBI_TypeC_SDA0	Display Bus Interface Type C Serial Data 0 (Only for BL618)
					24	-	DISP_QSPI_SCL	Display Quad SPI Serial Clock (Only for BL618)
					25	-	-	
					26	-	M0_JTAG_TDO	M0 JTAG Test Data Out

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
10	16	VDDIO_1	DI/DO	PAD_GPIO_11	0		SDH_DAT0	SD Host Data 0
					1	-	SPI_MOSI	SPI Master Output, Slave Input
					2	-	SF3_CLK	NOR FALSH controller signal3 Clock
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_11_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_11_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_11_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_11_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_11_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_11_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_11_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_11_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	CAM1_DAT2	Camera 1 Data 2 (Only for BL618)
					10	-	-	-
					11	-	SWGPIO11	Software GPIO 11
					12	-	SDIO_DAT3	SDIO Data 3
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0 Channel 1 Negative
					22	-	DBI_TypeB_DB3	Display Bus Interface Type B Data Bit 3 (Only for BL618)
					23	-	DBI_TypeC_DCn	Display Bus Interface Type C Data /Command Control (Only for BL618)
					24	-	DISP_QSPI_CSn	Display Quad SPI Chip Select (Only for BL618)
					25	-	-	-
					26	-	M0_JTAG_TDI	M0 JTAG Test Data Input

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
11	17	VDDIO_1	DI/DO	PAD_GPIO_12	0		SDH_CLK	SD Host Clock
					1	-	SPI_SS	SPI Slave Select
					2	-	SF3_D0	NOR FALSH controller signal3 Data0
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_0_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_0_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_0_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_0_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_0_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_0_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_0_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_0_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	CAM1_DAT3	Camera 1 Data 3 (Only for BL618)
					10	-	ADC_CH6	ADC Channel 6
					11	-	SWGPIO12	Software GPIO 12
					12	-	SDIO_CMD	SDIO Command
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0 Channel 2 Positive
					22	-	DBI_TypeB_DB4	Display Bus Interface Type B Data Bit 4 (Only for BL618)
					23	-	DBI_TypeC_SCL	Display Bus Interface Type C Serial Clock (Only for BL618)
					24	-	DISP_QSPI_SDA0	Display Quad SPI Serial Data 0 (Only for BL618)
					25	-	-	-
					26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
12	18	VDDIO_1	DI/DO	PAD_GPIO_13	0	-	SDH_CMD	SD Host Command
					1	-	SPI_SCLK	SPI Serial Clock
					2	-	SF3_D2	NOR FALSH controller signal3 Data2
					3	-	I2S_FS	I2S Frame Sync
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_1_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_1_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_1_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_1_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_1_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_1_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_1_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_1_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	CAM1_CLK	Camera 1 Clock (Only for BL618)
					10	-	ADC_CH5	ADC Channel 5
					11	-	SWGPIO13	Software GPIO 13
					12	-	SDIO_CLK	SDIO Clock
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0 Channel 2 Negative
					22	-	DBI_TypeB_DB5	Display Bus Interface Type B Data Bit 5 (Only for BL618)
					23	-	DBI_TypeC_CSn	Display Bus Interface Type C Chip Select (Only for BL618)
					24	-	DISP_QSPI_SDA1	Display Quad SPI Serial Data 1 (Only for BL618)
					25	-	-	-
					26	-	M0_JTAG_TCK	M0 JTAG Test Clock

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
13	19	VDDIO_1	DI/DO	PAD_GPIO_14	0		SDH_DAT3	SD Host Data 3
					1	-	SPI_MISO	SPI Master Input, Slave Output
					2	-	SF3_D1	NOR FALSH controller signal3 Data 1
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_2_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_2_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_2_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_2_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_2_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_2_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_2_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_2_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	CAM1_DAT4	Camera 1 Data 4 (Only for BL618)
					10	-	ADC_CH4	ADC Channel 4
					11	-	SWGPIO14	Software GPIO 14
					12	-	SDIO_DAT0	SDIO Data 0
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0 Channel 3 Positive
					22	-	DBI_TypeB_DB6	Display Bus Interface Type B Data Bit 6 (Only for BL618)
					23	-	DBI_TypeC_SDA0	DBI_TypeC_SDA0 (Only for BL618)
					24	-	DISP_QSPI_SDA2	Display Quad SPI Serial Data 2 (Only for BL618)
					25	-	AUDAC_PWM_P	AUDAC_PWM_P
					26	-	M0_JTAG_TDO	M0 JTAG Test Data Out

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
14	20	VDDIO_1	DI/DO	PAD_GPIO_15	0		SDH_DAT2	SD Host Data 2
					1	-	SPI_MOSI	SPI Master Output, Slave Input
					2	-	SF3_CS	NOR FALSH controller signal3 Chip Select
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_3_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_3_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_3_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_3_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_3_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_3_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_3_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_3_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	CAM1_DAT5	Camera 1 Data 5 (Only for BL618)
					10	-	-	-
					11	-	SWGPIO15	Software GPIO 15
					12	-	SDIO_DAT1	SDIO Data 1
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0 Channel 3 Negative
					22	-	DBI_TypeB_DB7	Display Bus Interface Type B Data Bit 7 (Only for BL618)
					23	-	DBI_TypeC_DCn	Display Bus Interface Type C Data /Command Control (Only for BL618)
					24	-	DISP_QSPI_SDA3	Display Quad SPI Serial Data 3 (Only for BL618)
					25	-	AUDAC_PWM_N	AUDAC_PWM_N
					26	-	M0_JTAG_TDI	M0 JTAG Test Data Input

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
					-	-	-	-
					1	-	SPI_SS	SPI Slave Select
					2	-	-	-
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_4_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_4_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_4_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_4_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_4_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_4_sel=5	UART1_CTS	UART 1 Clear To Send
15	21	AVDD33_AON	DI/DO	PAD_GPIO_16		uart_sig_4_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_4_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	CAM1_DAT6	Camera 1 Data 6 (Only for BL618)
					10	-	-	-
					11	-	SWGPIO16	Software GPIO 16
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0 Channel 0 Positive
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
16	22	AVDD33_AON	DI/DO	PAD_GPIO_17	0	-	-	-
					1	-	SPI_SCLK	SPI Serial Clock
					2	-	-	-
					3	-	I2S_FS	I2S Frame Sync
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_5_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_5_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_5_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_5_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_5_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_5_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_5_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_5_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	CAM1_DAT7	Camera 1 Data 7 (Only for BL618)
					10	-	-	-
					11	-	SWGPIO17	Software GPIO 17
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0 Channel 0 Negative
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TCK	M0 JTAG Test Clock

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	23	AVDD33_AON	DI/DO	PAD_GPIO_18	0	-	-	-
					1	-	SPI_MISO	SPI Master Input, Slave Output
					2	-	-	
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_6_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_6_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_6_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_6_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_6_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_6_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_6_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_6_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO18	Software GPIO 18
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0 Channel 1 Positive
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDO	M0 JTAG Test Data Out

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	24	AVDD33_AON	DI/DO	PAD_GPIO_19	0	-	-	-
					1	-	SPI_MOSI	SPI Master Output, Slave Input
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_7_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_7_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_7_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_7_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_7_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_7_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_7_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_7_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH1	ADC Channel 1
					11	-	SWGPIO19	Software GPIO 19
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0 Channel 1 Negative
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDI	M0 JTAG Test Data Input
17	25	AVDD33_AON	Analog	CHIP_EN			CHIP_EN	CHIP_EN
18	26	-	Power,Input	AVDD33_AON	-	-	AVDD33_AON	3.3V power supply for always-on circuits
19	27	-	Power,Output	VDD18_FLASH	-	-	VDD18_FLASH	1.8V/3.3V power supply for embeded FLASH /pSRAM (internal regulator output)
20	28	-	Power,Input	PVDD33_DCDC	-	-	PVDD33_DCDC	3.3V power supply for DCDC
21	29	-	Power,Output	SW_DCDC	-	-	SW_DCDC	Switch PIN of DCDC
22	30	-	Power,Inout	DCDC_OUT	-	-	DCDC_OUT	DCDC output
23	31	-	Power,Output	DVDD11	-	-	DVDD11	Power supply of digital core (internal regulator output)
24	32	-	Power,Input	VDDIO_USB	-	-	VDDIO_USB	3.3V power supply of USB and audadc
25	33	VDDIO_USB	DI/DO	USB_DP			USB_DP	USB_DP
26	34	VDDIO_USB	DI/DO	USB_DM			USB_DM	USB_DM

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
27	35	VDDIO_2	DI/DO	PAD_GPIO_20	0	-	-	-
					1	-	SPI_SS	SPI Slave Select
					2	-	-	-
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	PDM_CLK_O	PDM Clock Line
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_8_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_8_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_8_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_8_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_8_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_8_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_8_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_8_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	-	-
					10	-	ADC_CH0/AUADC_CH0	ADC Channel 0/ Audio ADC Channel 0 (Only for BL618)
					11	-	SWGPIO20	Software GPIO 20
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0 Channel 2 Positive
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
28	36	VDDIO_2	DI/DO	PAD_GPIO_21	0	-	-	-
					1	-	SPI_SCLK	SPI Serial Clock
					2	-	-	-
					3	-	I2S_FS	I2S Frame Sync
					4	-	PDM_0_IN	PDM Data Line
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_9_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_9_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_9_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_9_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_9_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_9_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_9_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_9_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO21	Software GPIO 21
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0 Channel 2 Negative
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TCK	M0 JTAG Test Clock

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
29	37	VDDIO_2	DI/DO	PAD_GPIO_22	0	-	-	-
					1	-	SPI_MISO	SPI Master Input, Slave Output
					2	-	-	
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_10_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_10_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_10_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_10_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_10_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_10_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_10_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_10_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	-	-
					10	-	-	-
					11	-	SWGPIO22	Software GPIO 22
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0 Channel 3 Positive
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	AUDAC_PWM_P	AUDAC_PWM_P
					26	-	M0_JTAG_TDO	M0 JTAG Test Data Out

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	38	VDDIO_2	DI/DO	PAD_GPIO_23	0	-	-	-
					1	-	SPI_MOSI	SPI Master Output, Slave Input
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_11_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_11_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_11_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_11_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_11_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_11_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_11_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_11_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	-	-
					10	-	AUADC_CH3	Audio ADC Channel 3(Only for BL618)
					11	-	SWGPIO23	Software GPIO 23
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0 Channel 3 Negative
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	AUDAC_PWM_N	AUDAC_PWM_N
					26	-	M0_JTAG_TDI	M0 JTAG Test Data Input

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	39	VDDIO_2	DI/DO	PAD_GPIO_24	0	-	-	-
					1	-	SPI_SS	SPI Slave Select
					2	-	-	-
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_0_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_0_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_0_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_0_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_0_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_0_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_0_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_0_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	-	-
					9	-	CAM0_DAT0	Camera 0 Data 0 (Only for BL618)
					10	-	-	-
					11	-	SWGPIO24	Software GPIO 24
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0 Channel 0 Positive
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	40	VDDIO_2	DI/DO	PAD_GPIO_25	0	-	-	-
					1	-	SPI_SCLK	SPI Serial Clock
					2	-	-	-
					3	-	I2S_FS	I2S Frame Sync
					4	-	PDM_0_IN	PDM Data Line
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_1_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_1_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_1_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_1_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_1_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_1_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_1_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_1_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	RMII_REF_CLK	RMII Reference Clock (Only for BL618)
					9	-	CAM0_DAT1	Camera 0 Data 1 (Only for BL618)
					10	-	-	-
					11	-	SWGPIO25	Software GPIO 25
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0 Channel 0 Negative
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TCK	M0 JTAG Test Clock

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	41	VDDIO_2	DI/DO	PAD_GPIO_26	0	-	-	-
					1	-	SPI_MISO	SPI Master Input, Slave Output
					2	-	-	
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	PDM_CLK_O	PDM Clock Line
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_2_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_2_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_2_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_2_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_2_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_2_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_2_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_2_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	RMII_TXD[0]	RMII Transmit Data[0] (Only for BL618)
					9	-	CAM0_DAT2	Camera 0 Data 2 (Only for BL618)
					10	-	-	-
					11	-	SWGPIO26	Software GPIO 26
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0 Channel 1 Positive
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDO	M0 JTAG Test Data Out

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
30	42	-	Power,Input	VDDIO2	-	-	VDDIO2	1.8V/3.3V power supply of GPIO20 - GPIO34
31	43	VDDIO_2	DI/DO	PAD_GPIO_27	0	-	-	-
					1	-	SPI_MOSI	SPI Master Output, Slave Input
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_3_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_3_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_3_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_3_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_3_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_3_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_3_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_3_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	RMII_TXD[1]	RMII Transmit Data[1] (Only for BL618)
					9	-	CAM0_DAT3	Camera 0 Data 3 (Only for BL618)
					10	-	ADC_CH10/AUADC_CH4	ADC Channel 10 /Audio ADC Channel 4 (Only for BL618)
					11	-	SWGPIO27	Software GPIO 27
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
						reg_pwm1_io_sel=1	PWM0_CH1N	PWM0 Channel 1 Negative
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	AUDAC_PWM_N	AUDAC_PWM_N
					26	-	M0_JTAG_TDI	M0 JTAG Test Data Input

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
32	44	VDDIO_2	DI/DO	PAD_GPIO_28	0	-	-	-
					1	-	SPI_SS	SPI Slave Select
					2	-	-	-
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_4_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_4_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_4_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_4_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_4_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_4_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_4_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_4_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	RMII_RXD[0]	RMII Receive Data[0] (Only for BL618)
					9	-	CAM0_HSYNC	Camera 0 Horizontal Sync (Only for BL618)
					10	-	-	-
					11	-	SWGPIO28	Software GPIO 28
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
						reg_pwm1_io_sel=1	PWM0_CH2P	PWM0 Channel 2 Positive
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	AUDAC_PWM_P	AUDAC_PWM_P
					26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
33	45	VDDIO_2	DI/DO	PAD_GPIO_29	0	-	-	-
					1	-	SPI_SCLK	SPI Serial Clock
					2	-	-	-
					3	-	I2S_FS	I2S Frame Sync
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_5_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_5_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_5_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_5_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_5_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_5_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_5_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_5_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	RMII_RXD[1]	RMII Receive Data[1] (Only for BL618)
					9	-	CAM0_VSYNC	Camera 0 Vertical Sync (Only for BL618)
					10	-	-	-
					11	-	SWGPIO29	Software GPIO 29
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
						reg_pwm1_io_sel=1	PWM0_CH2N	PWM0 Channel 2 Negative
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TCK	M0 JTAG Test Clock

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
34	46	VDDIO_2	DI/DO	PAD_GPIO_30	0	-	-	-
					1	-	SPI_MISO	SPI Master Input, Slave Output
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_6_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_6_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_6_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_6_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_6_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_6_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_6_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_6_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	RMII_RXERR	RMII Receive Error (Only for BL618)
					9	-	CAM0_CLK	Camera 0 Clock (Only for BL618)
					10	-	AUADC_CH7	Audio ADC Channel 7(Only for BL618)
					11	-	SWGPIO30	Software GPIO 30
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
						reg_pwm1_io_sel=1	PWM0_CH3P	PWM0 Channel 3 Positive
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDO	M0 JTAG Test Data Out

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	47	VDDIO_2	DI/DO	PAD_GPIO_31	0	-	-	-
					1	-	SPI_MOSI	SPI Master Output, Slave Input
					2	-	-	-
					3	-	I2S_DO/I2S_RCLK_O	I2S Data Output/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_7_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_7_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_7_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_7_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_7_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_7_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_7_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_7_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	RMII_TX_EN	RMII Transmit Enable (Only for BL618)
					9	-	CAM0_DAT4	Camera 0 Data 4 (Only for BL618)
					10	-	-	-
					11	-	SWGPIO31	Software GPIO 31
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH3P	PWM0 Channel 3 Positive
						reg_pwm1_io_sel=1	PWM0_CH3N	PWM0 Channel 3 Negative
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDI	M0 JTAG Test Data Input

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	48	VDDIO_2	DI/DO	PAD_GPIO_32	0	-	-	-
					1	-	SPI_SS	SPI Slave Select
					2	-	-	-
					3	-	I2S_BCLK	I2S Bit Clock
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_8_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_8_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_8_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_8_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_8_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_8_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_8_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_8_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	RMII_RX_DV	RMII Receive Data Valid (Only for BL618)
					9	-	CAM0_DAT5	Camera 0 Data 5 (Only for BL618)
					10	-	-	-
					11	-	SWGPIO32	Software GPIO 32
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH0P	PWM0 Channel 0 Positive
						reg_pwm1_io_sel=1	PWM0_CH0P	PWM0 Channel 0 Positive
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TMS	M0 JTAG Test Mode Select

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	49	VDDIO_2	DI/DO	PAD_GPIO_33	0	-	-	-
					1	-	SPI_SCLK	SPI Serial Clock
					2	-	-	-
					3	-	I2S_FS	I2S Frame Sync
					4	-	-	-
					5	-	I2C0_SDA	I2C 0 Serial Data
					6	-	I2C1_SDA	I2C 1 Serial Data
					7	uart_sig_9_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_9_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_9_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_9_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_9_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_9_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_9_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_9_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	RMII_MDC	RMII Management Data Clock (Only for BL618)
					9	-	CAM0_DAT6	Camera 0 Data 6 (Only for BL618)
					10	-	-	-
					11	-	SWGPIO33	Software GPIO 33
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH1P	PWM0 Channel 1 Positive
						reg_pwm1_io_sel=1	PWM0_CH0N	PWM0 Channel 0 Negative
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TCK	M0 JTAG Test Clock

表 3.1: 管脚定义 (continued)

BL616	BL618	Voltage Domain	Type	Pin Name	GPIO Function Select Number	Peripheral Internal Function Select	PAD Main Function	Description
-	50	VDDIO_2	DI/DO	PAD_GPIO_34	0	-	-	-
					1	-	SPI_MISO	SPI Master Input, Slave Output
					2	-	-	-
					3	-	I2S_DI/I2S_RCLK_O	I2S Data Input/I2S Receive Clock Output
					4	-	-	-
					5	-	I2C0_SCL	I2C 0 Serial Clock
					6	-	I2C1_SCL	I2C 1 Serial Clock
					7	uart_sig_10_sel=0	UART0_RTS	UART 0 Request To Send
						uart_sig_10_sel=1	UART0_CTS	UART 0 Clear To Send
						uart_sig_10_sel=2	UART0_TXD	UART 0 Transmit Data
						uart_sig_10_sel=3	UART0_RXD	UART 0 Receive Data
						uart_sig_10_sel=4	UART1_RTS	UART 1 Request To Send
						uart_sig_10_sel=5	UART1_CTS	UART 1 Clear To Send
						uart_sig_10_sel=6	UART1_TXD	UART 1 Transmit Data
						uart_sig_10_sel=7	UART1_RXD	UART 1 Receive Data
					8	-	RMII_MDIO	RMII Management Data Input/Output (Only for BL618)
					9	-	CAM0_DAT7	Camera 0 Data 7 (Only for BL618)
					10	-	-	-
					11	-	SWGPIO34	Software GPIO 34
					12	-	-	-
					16	reg_pwm1_io_sel=0	PWM0_CH2P	PWM0 Channel 2 Positive
						reg_pwm1_io_sel=1	PWM0_CH1P	PWM0 Channel 1 Positive
					22	-	-	-
					23	-	-	-
					24	-	-	-
					25	-	-	-
					26	-	M0_JTAG_TDO	M0 JTAG Test Data Out
35	51	AVDD33_RF3	Clock	XTAL_IN			XTAL_IN	
36	52	AVDD33_RF3	Clock	XTAL_OUT			XTAL_OUT	
37	53	-	Power,Input	AVDD33_RF3	-	-	AVDD33_RF3	3.3V power supply of RF transceiver
38	54	-	Power,Input	AVDD18_RF	-	-	AVDD18_RF	1.8V power supply of RF transceiver
39	55	-	Power,Output	AVDD15_RF2	-	-	AVDD15_RF2	1.5V power supply of RF transceiver (internal regulator output)
40	56	-	Power,Input	AVDD15_RF1	-	-	AVDD15_RF1	1.5V power supply of RF transceiver

1 CAM0 和 CAM1 只能选择一个。

2 当选为 SPI 功能时，默认为 SPI_MISO，可通过寄存器将该功能转换为 SPI_MOSI。

3 SF1 用于内部 flash，SF2 和 SF3 不能同时使用。

3.1 电源框图

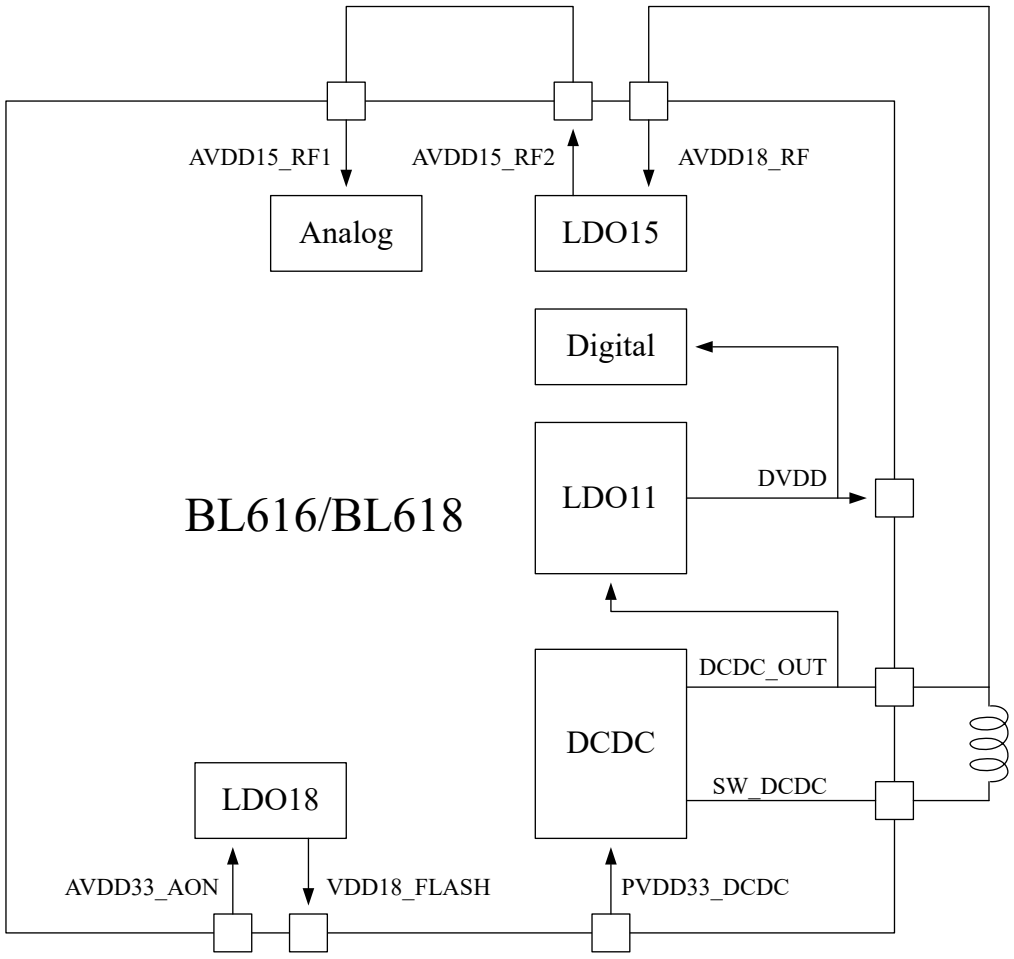

图 3.3: 电源框图

4 音频特性 (Only for BL618)

表 4.1: AUADC 性能

At 25°C, VDDIO= 3.3 V, f_S= 48kHz, 16-bit audio data (unless otherwise noted)						
参数		测试条件	最小值	典型值	最大值	单位
AUDIO ADC	Input signal full-scale level	differential input，6dB PGA gain		1.16		Vrms
		Single-ended input，6dB PGA gain		0.8		
	Input common-mode voltage	differential/Single-ended input		1.57		V
SNR	Signal-to-noise ratio, A-weighted	f_S= 48 kHz, 0 dB PGA gain, 1kHz full-scale sine-wave input		96		dB
DR	Dynamic range, A-weighted	f_S= 48 kHz, 0 dB PGA gain, 1kHz -60dB sine-wave input		95		
THD	Total harmonic distortion	f_S= 48 kHz, 0 dB PGA gain, 1kHz -5dB sine-wave input		-90		
Freq. Response(20Hz~16kHz)		-5dB sine-wave input		±0.13		
ADC programmable analogue amplifier gain range		Analogue gain resolution = 3dB	6		42	
ADC programmable digital gain range		Digital gain resolution = 0.5dB	-95.5		31.5	
Input resistance		Analogue gain 6dB~42dB	160K		480	kΩ

表 4.2: AUDAC 性能

At 25°C, VDDIO= 3.3 V, f_S= 48kHz, @AUDAC_P/N with RC filter(R=1KΩ , C=470pF) (unless otherwise noted)						
参数		测试条件	最小值	典型值	最大值	单位
AUDIO DAC	Input signal full-scale level	Differential output，0 dB line-out gain		1.8		Vrms

表 4.2: AUDAC 性能 (continued)

At 25°C, VDDIO= 3.3 V, f_S= 48kHz, @AUDAC_P/N with RC filter(R=1KΩ , C=470pF) (unless otherwise noted)						
参数		测试条件	最小值	典型值	最大值	单位
SNR	Signal-to-noise ratio, A-Weighted	f_S= 48 kHz, 1kHz full-scale sine-wave output		95		dB
DR	Dynamic range, A-weighted	f_S= 48 kHz, 1kHz -60dB sine-wave output		95		
THD	Total harmonic distortion	f_S= 48 kHz, 1kHz -5dB sine-wave output		-80		
Noise Floor		Play 0data @ No A-weighted		26		Vrms
Freq. Response(20Hz~16kHz)		-5dB sine-wave input		±0.25		dB
programmable digital gain range		Digital gain resolution = 0.5dB	-95.5		31.5	

5 电气特性

5.1 绝对最大额定值

表 5.1: 电源的绝对最大额定值

管脚名称	最小值	最大值	单位
AVDD33_RF1, AVDD33_RF2, AVDD33_AON, PVDD33_DCDC, VDDIO_USB, AVDD33_RF3	-0.3	3.63	V
VDDIO1, VDDIO2	-0.3	3.63	V
ESD Protection (HBM)		2000	V
Storage Temperature	-45	135	°C

5.2 运行条件

5.2.1 电源特性

表 5.2: 建议电源值范围

管脚名称	最小值	典型值	最大值	单位
AVDD33_RF1, AVDD33_RF2, AVDD33_AON, PVDD33_DCDC, VDDIO_USB, AVDD33_RF3	2.97	3.3	3.63	V
VDDIO1, VDDIO2	2.97/1.62	3.3/1.8	3.63/1.98	

5.2.2 IO 直流特性

测试条件：IO 供电 VDDIO = 3.3V，温度 25°C

表 5.3: IO 直流特性

符号	描述	GPIO 号	条件	最小值	典型值	最大值	单位
VOH	Output voltage high	GPIO 21-22, GPIO28-29	GPIO drive strength 0, source current = 2.8mA		0.9*VDDIO		V
			GPIO drive strength 1, source current = 9.5mA				
			GPIO drive strength 2, source current = 17.4mA				
			GPIO drive strength 3, source current = 23.8mA				
		GPIO 0-20, GPIO 23-27, GPIO 30-34	GPIO drive strength 0, source current = 2.9mA				
			GPIO drive strength 1, source current = 8.5mA				
			GPIO drive strength 2, source current = 16.8mA				
			GPIO drive strength 3, source current = 22.2mA				
VOL	Output voltage low	GPIO 21-22, GPIO28-29	GPIO drive strength 0, sink current = 3.4mA		0.1*VDDIO		V
			GPIO drive strength 1, sink current = 10.2mA				
			GPIO drive strength 2, sink current = 20mA				
			GPIO drive strength 3, sink current = 26.5mA				
		GPIO 0-20, GPIO 23-27, GPIO 30-34	GPIO drive strength 0, sink current = 3.1mA				
			GPIO drive strength 1, sink current = 9.2mA				
			GPIO drive strength 2, sink current = 18.2mA				
			GPIO drive strength 3, sink current = 24mA				
VIH	Input voltage high			0.7*VDDIO			V
VIL	Input voltage low					0.3*VDDIO	V

5.2.3 上电时序

为确保正常的上电启动，电源、复位、Bootstrap 引脚需要满足相应的时序要求。

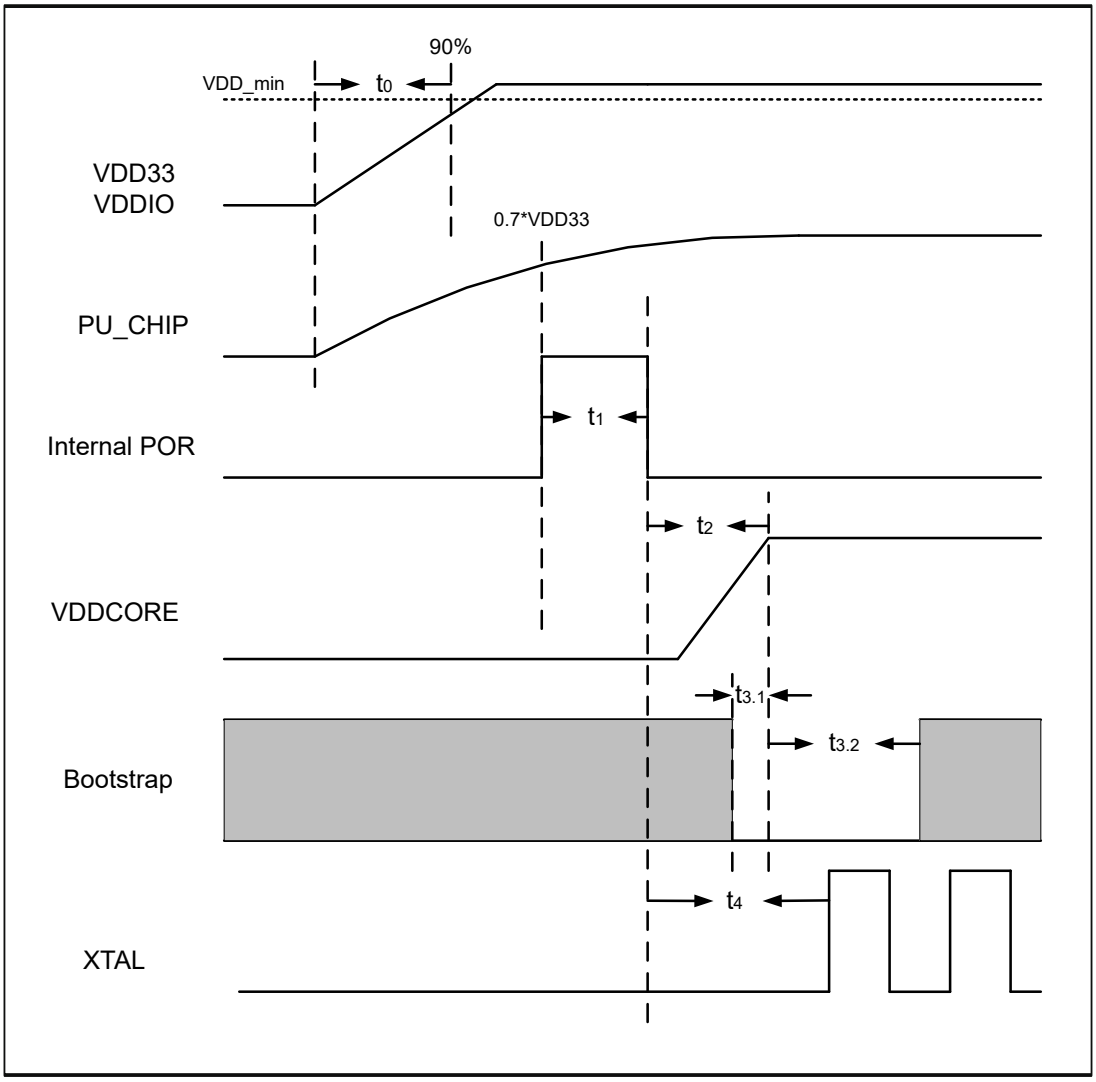

图 5.1: 上电时序

表 5.4: 上电时序参数说明

参数	说明	最小值 (ms)	典型值 (ms)	最大值 (ms)
t_0	电源电压到达 90% 的上升时间 [1]		0.1	
t_1	内部 POR 持续时间		3	
t_2	POR 变低到 VDDCORE 输出的时间		1	
$t_{3.1}$	Boostrap 引脚 [2]在 VDDCORE 建立前的准备时间	0		
$t_{3.2}$	Bootstrap 引脚保持有效电平的时间	2		
t_4	POR 变低到 XTAL 起振时间		1	

[1] VDD_min 是保证芯片正常工作的最小值。

[2] Bootstrap 引脚是 GPIO2。

5.2.4 复位时序

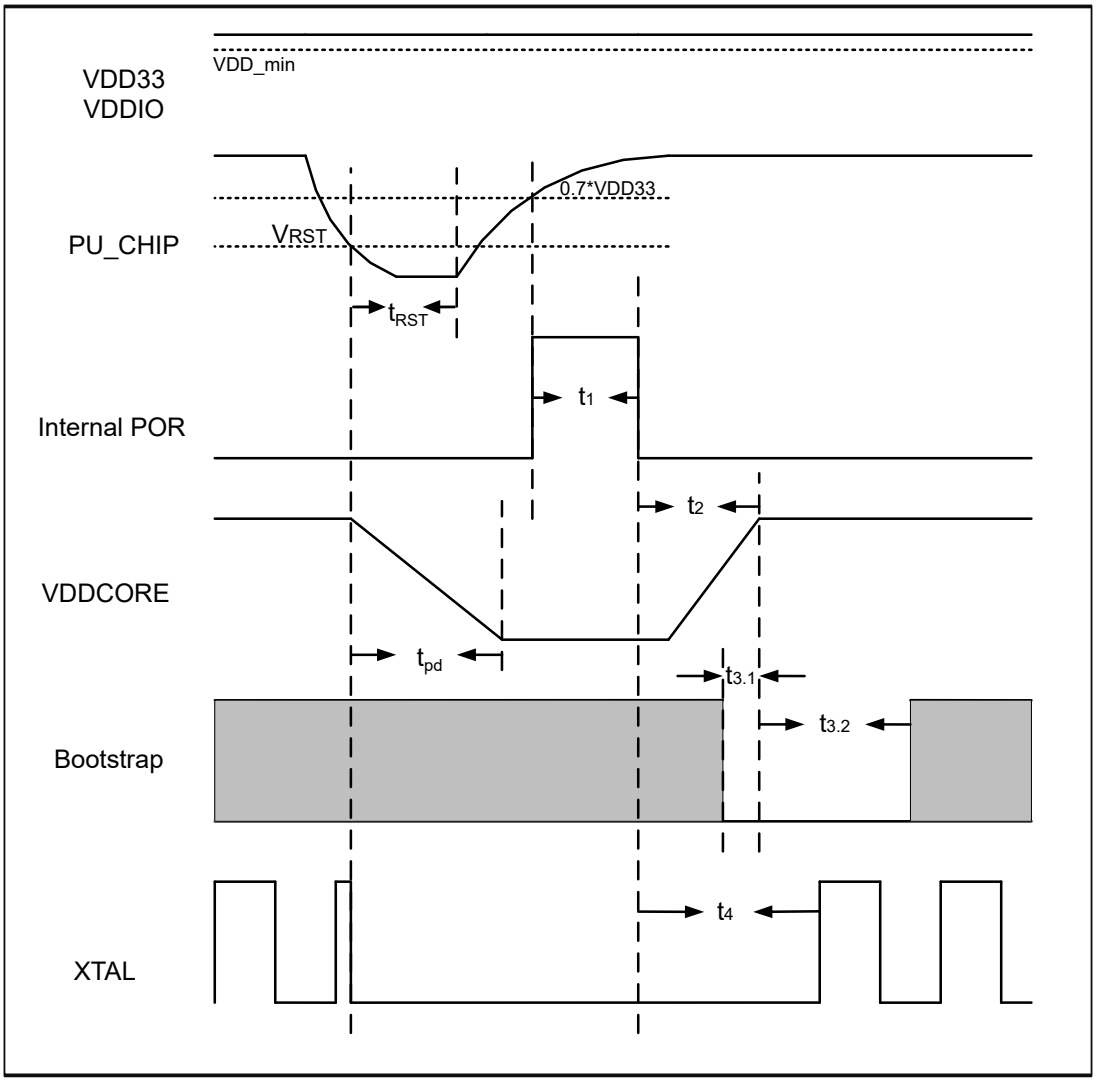

图 5.2: 复位时序

表 5.5: 复位时序参数说明

参数	说明	最小值	典型值	最大值	单位
V_{RST}	PU_CHIP 低于该值才会关机	0	0.1*VDD33	0.3*VDD33	V
t_{RST}	PU_CHIP 低于 VRST 的时间	1	1		ms
t_{pd}	关机后 VDDCORE 降低到 0 的时间	1	1		ms

5.2.5 温度特性

表 5.6: 温度特性

项目		最小值	典型值	最大值	单位
Ta	主芯片环境温度	-40		105	°C
	合封多芯片环境温度	-40		85	°C
Tj	结温度	-40		125	°C

表 5.7: Thermal Characteristics

Parameter Comments		Comments	Typ	Unit
θ_{JA}	Thermal resistance, J-to-A	Junction-to-ambient (still air) [1]	38	°C/W

[1] package mounted on 4LPCB using Finite Differential Modeling (FDM) method.

5.2.6 通用工作条件

表 5.8: 一般操作条件

项目	描述	最小值	典型值	最大值	单位
FCPU	CPU/TCM/Cache 时钟频率		320		MHz
FBUS	系统总线时钟频率		80		MHz

5.2.7 GPADC 特性

表 5.9: GPADC 特性

符号	参数	条件	最小值	典型值	最大值	单位
VDD	Supply voltage		2.3		3.6	V
T	Working tempreture		-40		125	°C
I_{vdd}	Current consumption	PGA1&2 off (2M clock)		150		μA
		PGA1&2 on(2M clock)		350		
Fclk	ADC input top clock frequency	Clock from SOC	1.5		32	MHz

表 5.9: GPADC 特性 (continued)

符号	参数	条件	最小值	典型值	最大值	单位
Fsample	Sampling rate	2M(12bit mode) 31.25K-125K(14bit mode) 7.8125K-15.625K(16bit mode)			1	MHz
Vin	Input voltage range	Differential mode			5.8	V(vpp)
		Single-ended mode			2.9	
Rin	Total input channel resistance				2	KΩ
Tpu	Power up time				1	uS
Tconv	Total conversion time	12bit mode			1	1/Fsample
		14bit mode [1]			16	
		14bit mode [2]			64	
		16bit mode [3]			128	
		16bit mode [4]			256	

[1] 14-bit mode with 16 times average
[2] 14-bit mode with 64 times average
[3] 16-bit mode with 128 times average
[4] 16-bit mode with 256 times average

表 5.10: ADC electrical characteristic

符号	参数	条件	最小值	典型值	最大值	单位
DNL [1]	Differential linearity error				+/-1	LSB
INL [1]	Integral linearity error				+/-2	LSB
Offset	Input offset				+/-2	LSB
Ge [1& 2]	Gain error				+/-1	%
ENOB	Effective number of bits	12bit mode(201KHz input)	9.7	10.5		bit
		14bit mode(2.5KHz input)	10.8	11.4		
		16bit mode(1KHz input)	11.5	12.3		
SNDR	Signal-to-noise-distortion (PGA on)	12bit mode(201KHz input)	59	65		dB
		14bit mode(2.5KHz input)	66	72.4		
		16bit mode(1KHz input)	71	76.8		
SNDR	Signal-to-noise-distortion (PGA gain=4)	12bit mode(201KHz input)	58	64		dB
		14bit mode(2.5KHz input)	64	69.5		
		16bit mode(1KHz input)	70	74		

[1] more test needed
[2] after calibration

6 产品使用

6.1 湿敏等级 (MSL)

芯片的湿敏等级为：MSL3。真空包装打开后，在 ≤30°C/60%RH 下，需要在 168 小时（7 天）内使用完毕，否则需要烘烤后上线。烘烤温度和时间可参考 IPC/JEDECJ-STD-033B01。

表 6.1: Reference Conditions for Drying Mounted or Unmounted SMD Packages (User Bake: Floor life begins counting at time = 0 after bake)

Package Body	Level	Bake @ 125°C		Bake @ 90°C ≤5% RH		Bake @ 40°C ≤5% RH	
		Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h	Exceeding Floor Life by >72 h	Exceeding Floor Life by ≤72 h
Thickness ≤1.4 mm	2	5 hours	3 hours	17 hours	11 hours	8 days	5 days
	2a	7 hours	5 hours	23 hours	13 hours	9 days	7 days
	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days
	4	11 hours	7 hours	37 hours	23 hours	15 days	9 days
	5	12 hours	7 hours	41 hours	24 hours	17 days	10 days
	5a	16 hours	10 hours	54 hours	24 hours	22 days	10 days

6.2 静电放电（ESD）

- 人体放电模式 (HBM): 2000V
- 组件充电模式 (CDM): 500V

6.3 回流焊接曲线 (Reflow Profile)

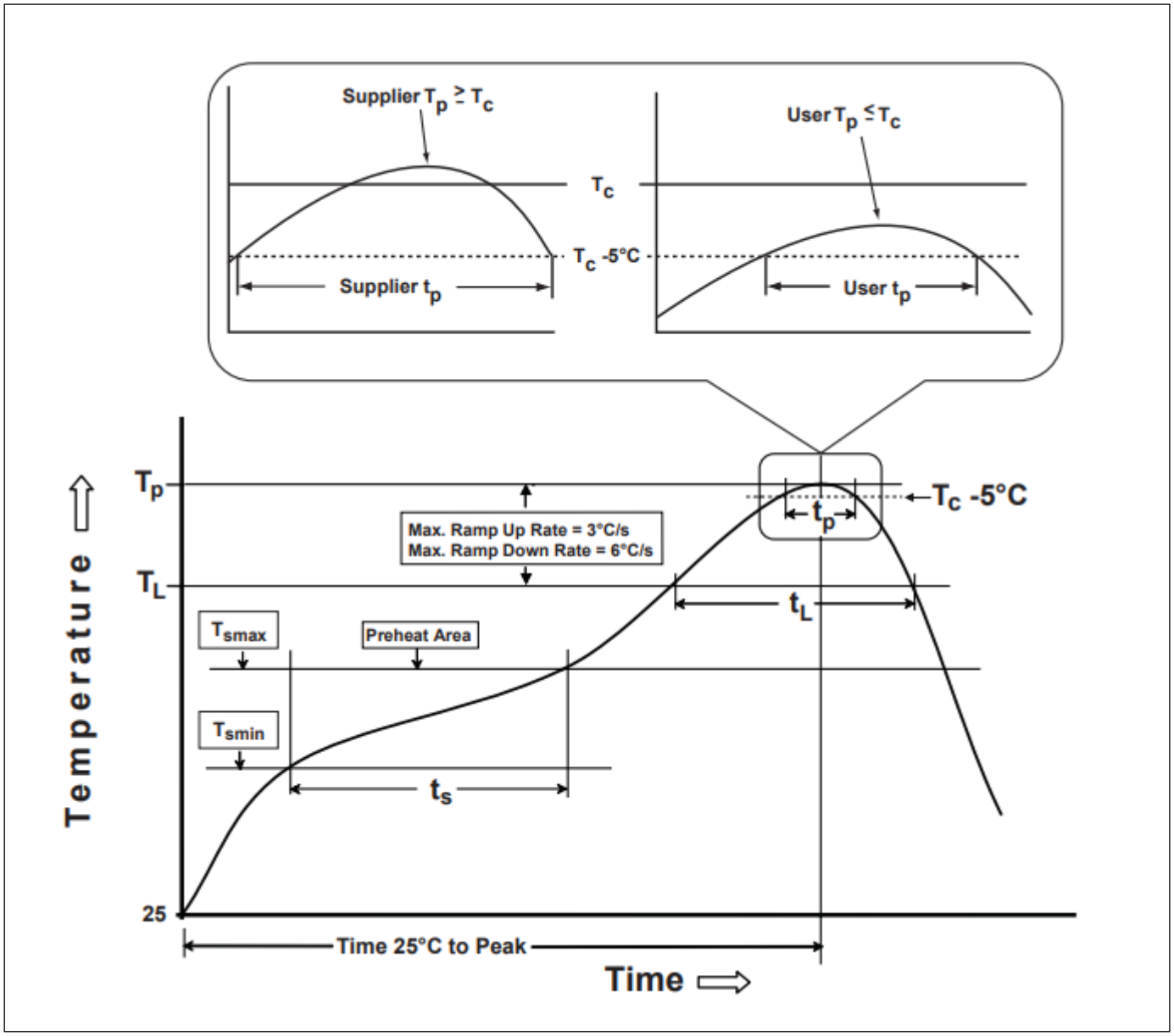

图 6.1: Classification Profile (Not to scale)

表 6.2: Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)	240 °C+0/-5 °C	250 °C+0/-5 °C
Time (t_p)* within 5 °C of the specified classification temperature (T_c)	10-30 seconds	20-40 seconds
Ramp-down rate (T_p to T_L)	6 °C/second max	6 °C/second max
Time 25 °C to peak temperature	6 minutes max	8 minutes max
- Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.		

具体可参考 IPC/JEDEC J-STD-020E。

7 参考设计

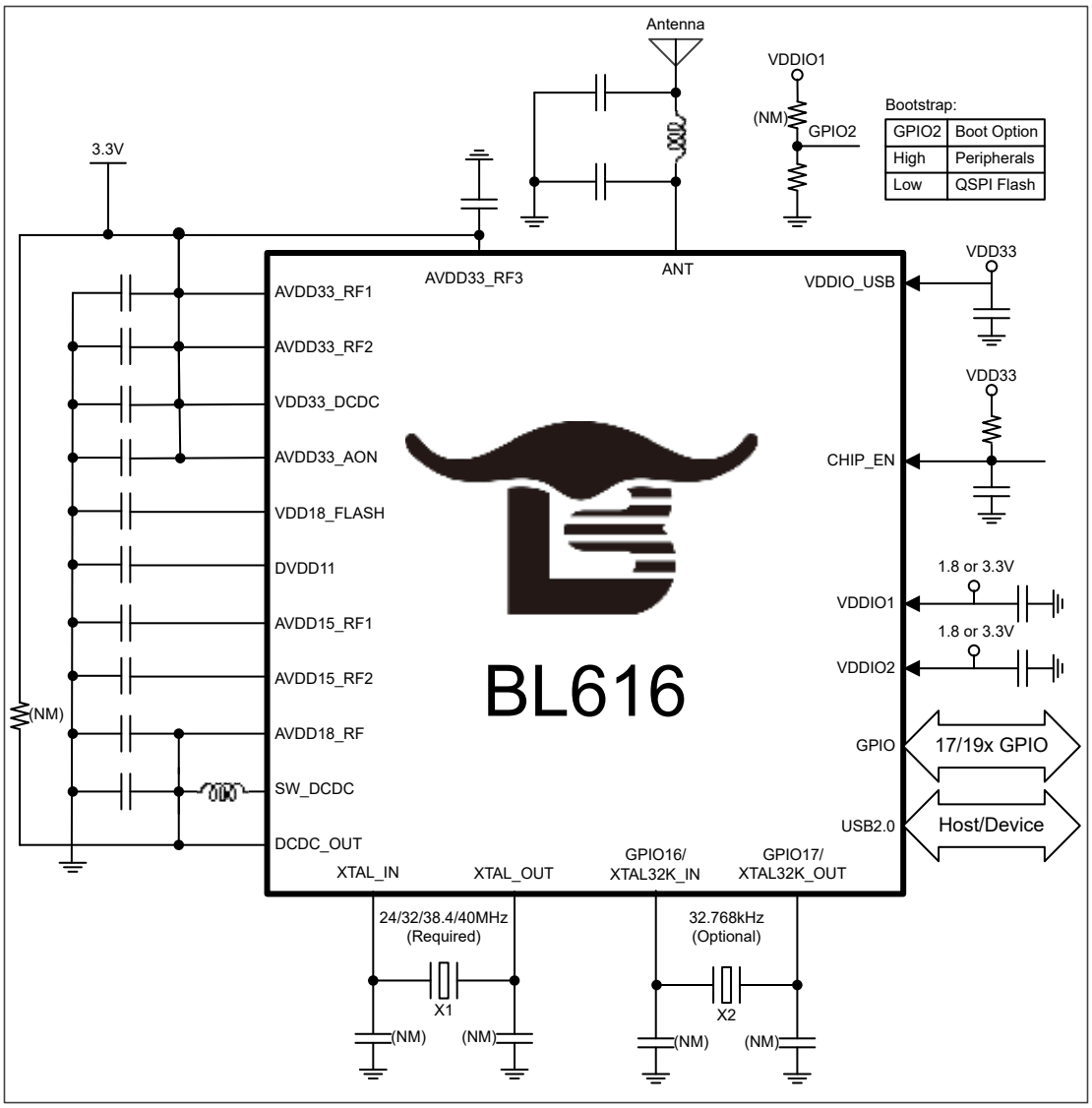

图 7.1: BL616 参考设计

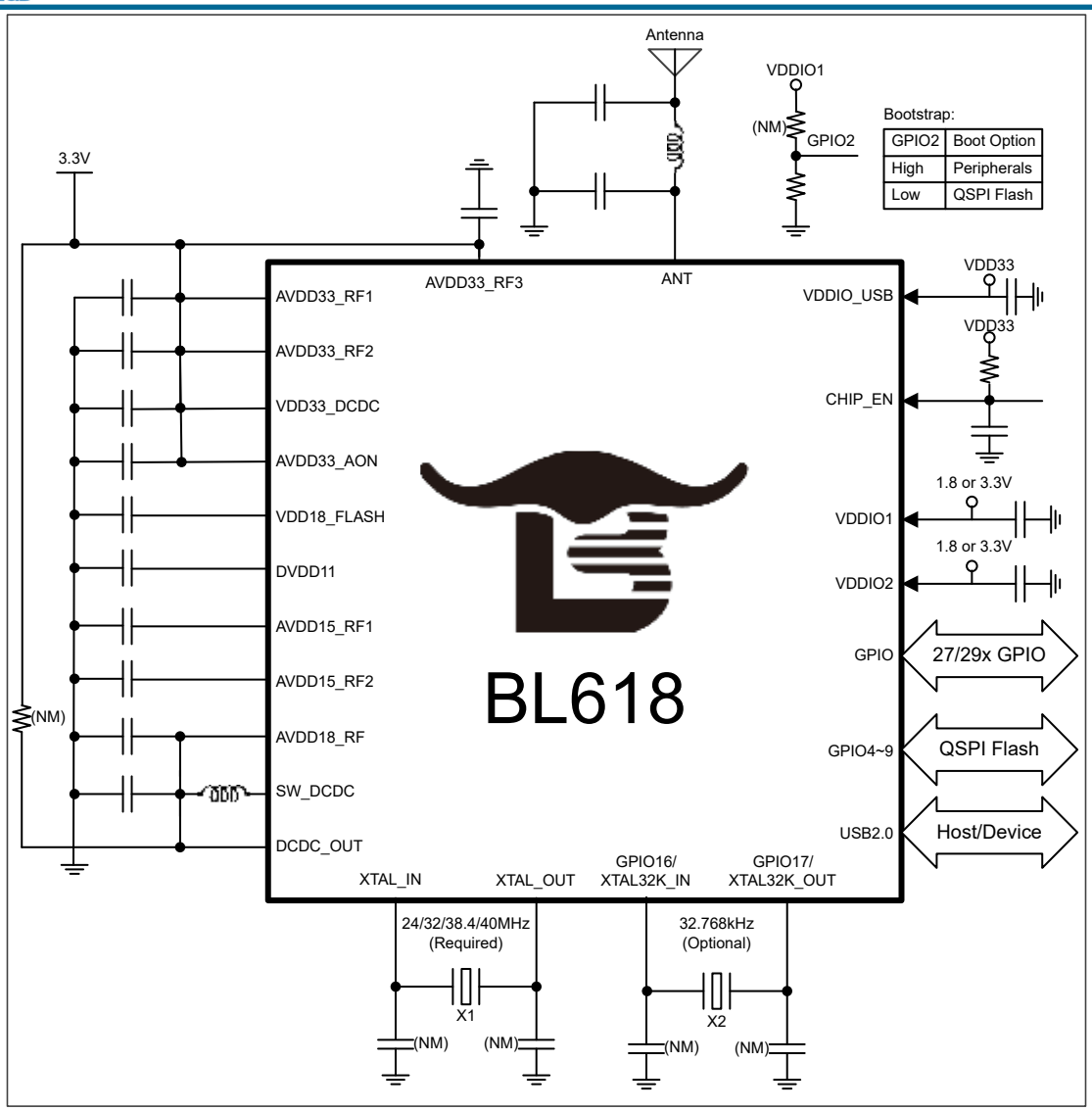

图 7.2: BL618 参考设计

8 封装信息 QFN40

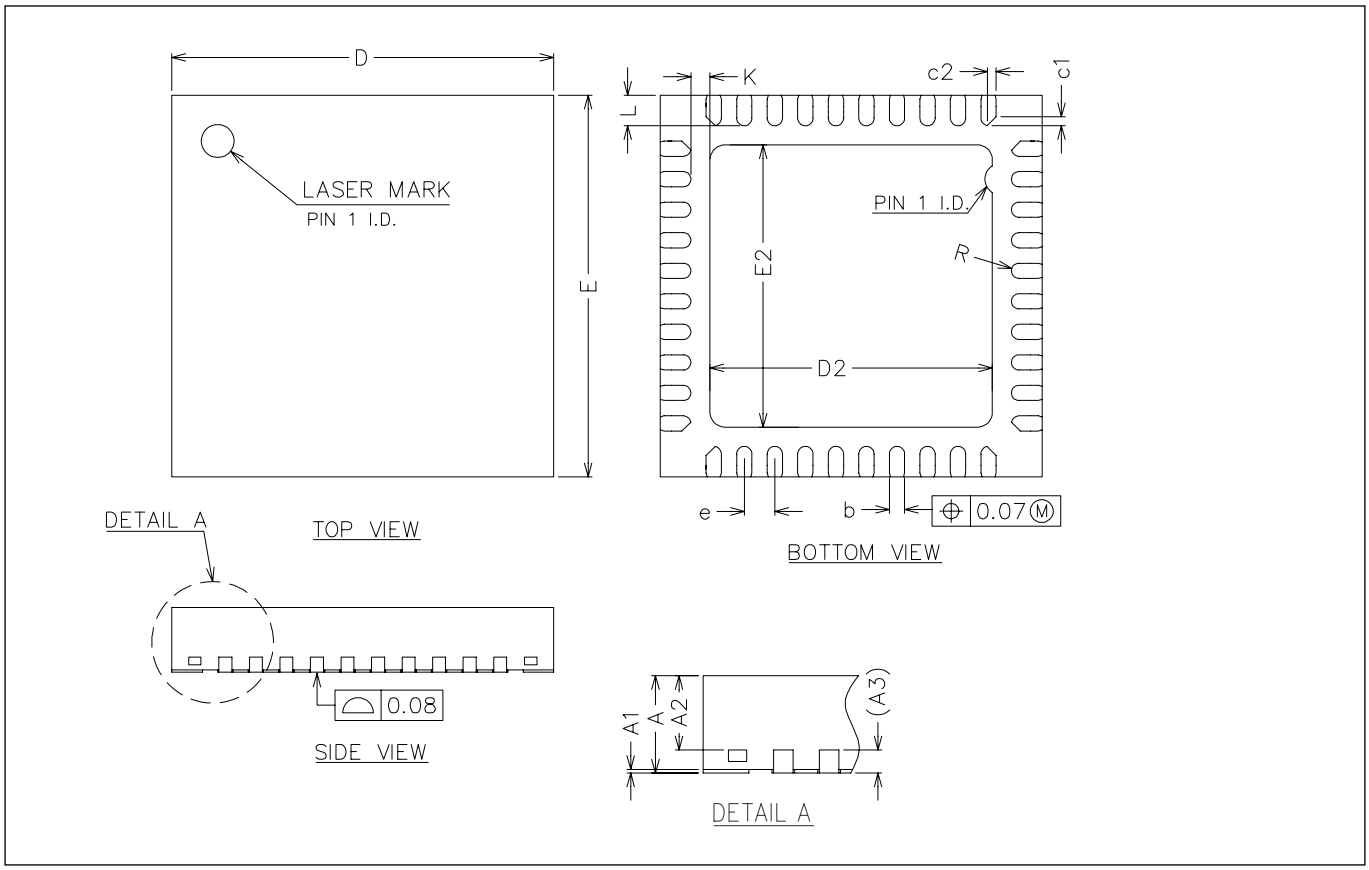

图 8.1: QFN40 封装图

表 8.1: QFN40 尺寸说明

标号	测量单位：毫米		
	最小值	典型值	最大值
A	0.80	0.85	0.90

表 8.1: QFN40 尺寸说明 (continued)

标号	测量单位：毫米		
	最小值	典型值	最大值
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3	0.20 REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	-	-
L	0.35	0.40	0.45
R	0.075	-	-
c1	-	0.12	-
c2	-	0.12	-

9 封装信息 QFN56

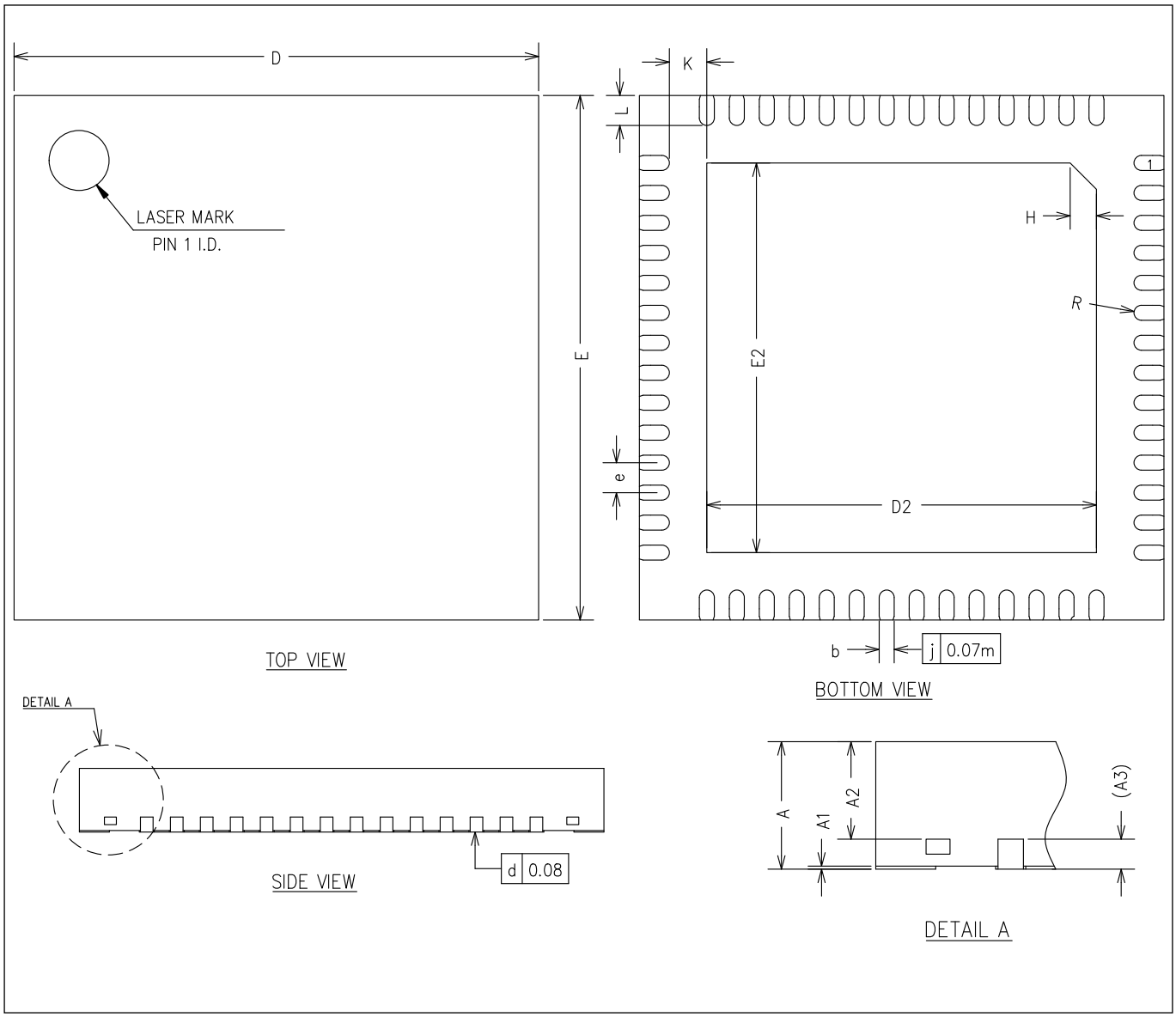

图 9.1: QFN56 封装图

表 9.1: QFN56 尺寸说明

标号	测量单位：毫米		
	最小值	典型值	最大值
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A2	0.60	0.65	0.70
A3	0.20 REF		
b	0.15	0.20	0.25
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.10	5.20	5.30
E2	5.10	5.20	5.30
e	0.30	0.40	0.50
H	0.35 REF		
K	0.50 REF		
L	0.35	0.40	0.45
R	0.09	-	-

10 标志定义

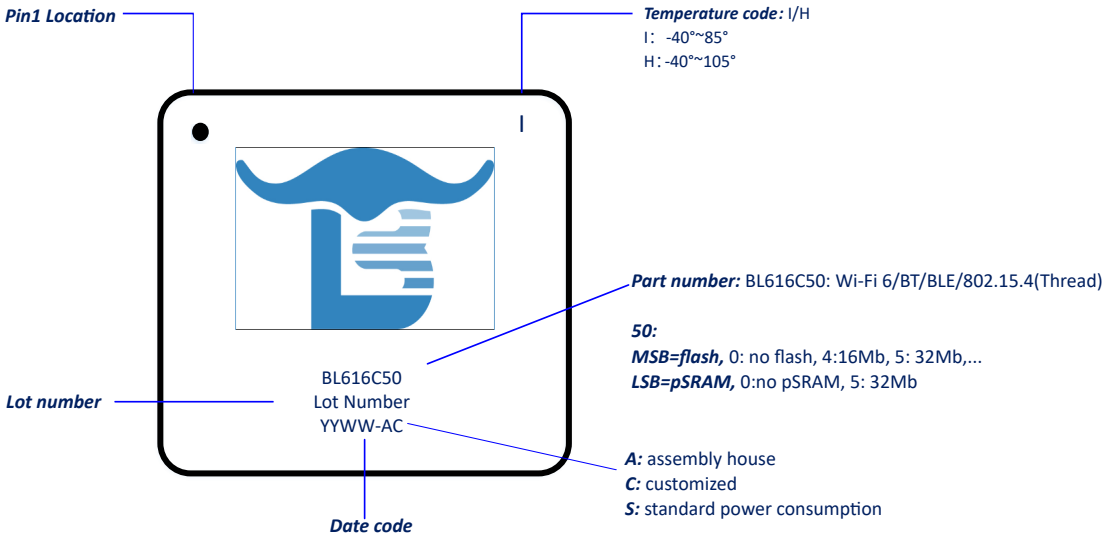

图 10.1: 标志定义

11 订购信息

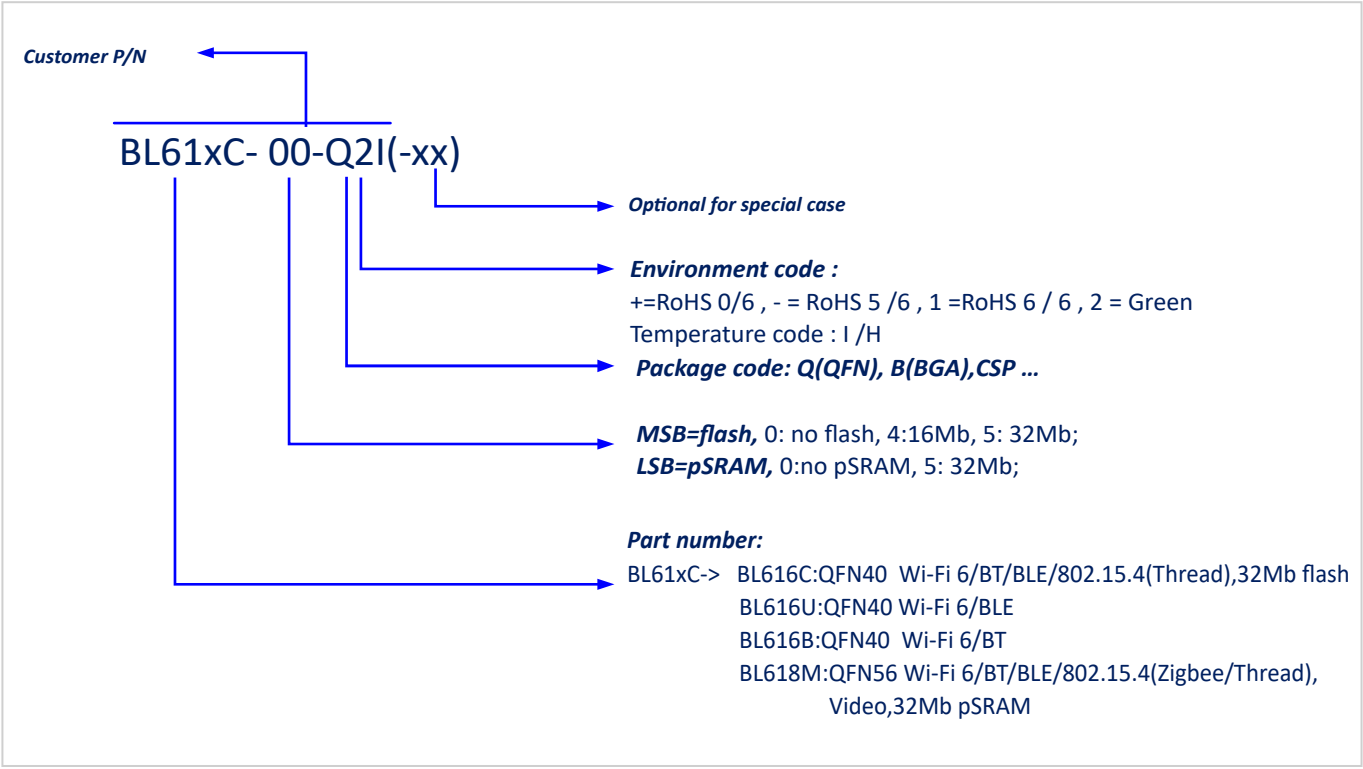

图 11.1: 型号命名

表 11.1: 订购选项

Customer P/N	Type	Package Size(mm)	MOQ	Description
BL616C-50-Q2I	QFN40	5x5x0.85, Pitch 0.4	6K	Wi-Fi 6/BT/BLE/802.15.4, 32Mb flash
BL616C-50-Q2IS	QFN40	5x5x0.85, Pitch 0.4	6K	Wi-Fi 6/BT/BLE/802.15.4, 32Mb flash, standard power consumption
BL618M-05-Q2I	QFN56	7x7x0.85, Pitch 0.4	3K	Wi-Fi 6/BT/BLE/802.15.4(Zigbee/Thread), Video, 32Mb pSRAM
BL618M-50-Q2I	QFN56	7x7x0.85, Pitch 0.4	3K	Wi-Fi 6/BT/BLE/802.15.4(Zigbee/Thread), Video, 32Mb flash

表 11.1: 订购选项 (continued)

Customer P/N	Type	Package Size(mm)	MOQ	Description
BL618M-65-Q2I	QFN56	7x7x0.85, Pitch 0.4	3K	Wi-Fi 6/BT/BLE/802.15.4(Zigbee/Thread), Video, 64Mb flash, 32Mb pSRAM

表 11.2: 产品包装信息

Package Size(mm)	Reel size	Quantity per Master Carton	Quantity per Roll	Reel Diameter	Tape Width	Tape Pitch	Moisture Sensitivity Level	Package Type
QFN 5*5	13”	30000	6000	330mm	12mm	8mm	MSL3	Tape reel
QFN 7*7	13”	15000	3000	330mm	16mm	12mm	MSL3	

12 版本信息

表 12.1: 修改记录

日期	版本	修改内容
2022/3/10	0.9	初版
2022/5/12	0.92	增加封装信息和标志定义
2022/5/18	0.93	增加 EMAC 时序说明
2022/6/7	0.94	增加电气特性和订购信息
2022/8/9	0.95	增加音频特性
2022/8/18	0.96	增加 spi 和 uart function 描述，型号命名中增加具体温度描述
2022/8/26	1.0	修改订购信息
2023/2/7	1.1	订购信息增加 BL616S-50-Q2I 描述
2023/3/14	1.2	增加 Audio 模块描述
2023/3/21	1.3	删除 GPIO21/22/28/29 模拟功能
2023/3/27	1.4	增加 GPADC 模块描述
2023/5/10	1.5	更新时钟树框图
2023/5/19	1.6	管脚定义表格中添加 AUADC 功能引脚描述
2023/6/25	1.7	添加 BL618M-50-Q2I 订购信息
2023/10/23	1.9	修改 GPIO 模拟功能描述
2023/11/3	2.0	区分 BL616 和 BL618 的功能差异
2023/11/9	2.1	1. 更新射频特性，更新温度特性 2. 更新功耗信息 3. 增加参考设计 4. 增加 SDIO 时序图，更新管脚功能描述
2023/12/22	2.2	增加 BL618M-65-Q2I 和 BL616C-50-Q2IS

表 12.1: 修改记录 (continued)

日期	版本	修改内容
2024/3/6	2.3	修改 EMAC 特性
2024/5/22	2.4	更新 GPADC 特性
2024/5/28	2.5	增加产品包装信息