

ESP32-WROOM-32

Datasheet



Version 2.8
Espressif Systems
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About This Document

This document provides the specifications for the ESP32-WROOM-32 module.

Revision History

For revision history of this document, please refer to the [last page](#).

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1. Overview

ESP32-WROOM-32 is a powerful, generic Wi-Fi+BT+BLE MCU module that targets a wide variety of applications, ranging from low-power sensor networks to the most demanding tasks, such as voice encoding, music streaming and MP3 decoding.

At the core of this module is the ESP32-D0WDQ6 chip*. The chip embedded is designed to be scalable and adaptive. There are two CPU cores that can be individually controlled, and the CPU clock frequency is adjustable from 80 MHz to 240 MHz. The user may also power off the CPU and make use of the low-power co-processor to constantly monitor the peripherals for changes or crossing of thresholds. ESP32 integrates a rich set of peripherals, ranging from capacitive touch sensors, Hall sensors, SD card interface, Ethernet, high-speed SPI, UART, I²S and I²C.

Note:

* For details on the part numbers of the ESP32 family of chips, please refer to the document [ESP32 Datasheet](#).

The integration of Bluetooth, Bluetooth LE and Wi-Fi ensures that a wide range of applications can be targeted, and that the module is all-around: using Wi-Fi allows a large physical range and direct connection to the Internet through a Wi-Fi router, while using Bluetooth allows the user to conveniently connect to the phone or broadcast low energy beacons for its detection. The sleep current of the ESP32 chip is less than 5 μ A, making it suitable for battery powered and wearable electronics applications. The module supports a data rate of up to 150 Mbps, and 20 dBm output power at the antenna to ensure the widest physical range. As such the module does offer industry-leading specifications and the best performance for electronic integration, range, power consumption, and connectivity.

The operating system chosen for ESP32 is freeRTOS with LwIP; TLS 1.2 with hardware acceleration is built in as well. Secure (encrypted) over the air (OTA) upgrade is also supported, so that users can upgrade their products even after their release, at minimum cost and effort.

Table 1 provides the specifications of ESP32-WROOM-32.

Table 1: ESP32-WROOM-32 Specifications

| Categories | Items | Specifications |
|---------------|-------------------------|--|
| Certification | RF certification | FCC/CE-RED/IC/TELEC/KCC/SRRC/NCC |
| | Wi-Fi certification | Wi-Fi Alliance |
| | Bluetooth certification | BQB |
| | Green certification | RoHS/REACH |
| Test | Reliability | HTOL/HTSL/uHAST/TCT/ESD |
| Wi-Fi | Protocols | 802.11 b/g/n (802.11n up to 150 Mbps) |
| | | A-MPDU and A-MSDU aggregation and 0.4 μ s guard interval support |
| | Frequency range | 2.4 GHz ~ 2.5 GHz |
| Bluetooth | Protocols | Bluetooth v4.2 BR/EDR and BLE specification |
| | | NZIF receiver with -97 dBm sensitivity |
| | Radio | Class-1, class-2 and class-3 transmitter |
| | | AFH |

| Categories | Items | Specifications |
|------------|---|--|
| | Audio | CVSD and SBC |
| Hardware | Module interfaces | SD card, UART, SPI, SDIO, I ² C, LED PWM, Motor PWM, I ² S, IR, pulse counter, GPIO, capacitive touch sensor, ADC, DAC |
| | On-chip sensor | Hall sensor |
| | Integrated crystal | 40 MHz crystal |
| | Integrated SPI flash | 4 MB |
| | Operating voltage/Power supply | 2.7 V ~ 3.6 V |
| | Operating current | Average: 80 mA |
| | Minimum current delivered by power supply | 500 mA |
| | Recommended operating temperature range | -40 °C ~ +85 °C |
| | Package size | (18.00±0.10) mm × (25.50±0.10) mm × (3.10±0.10) mm |

2. Pin Definitions

2.1 Pin Layout

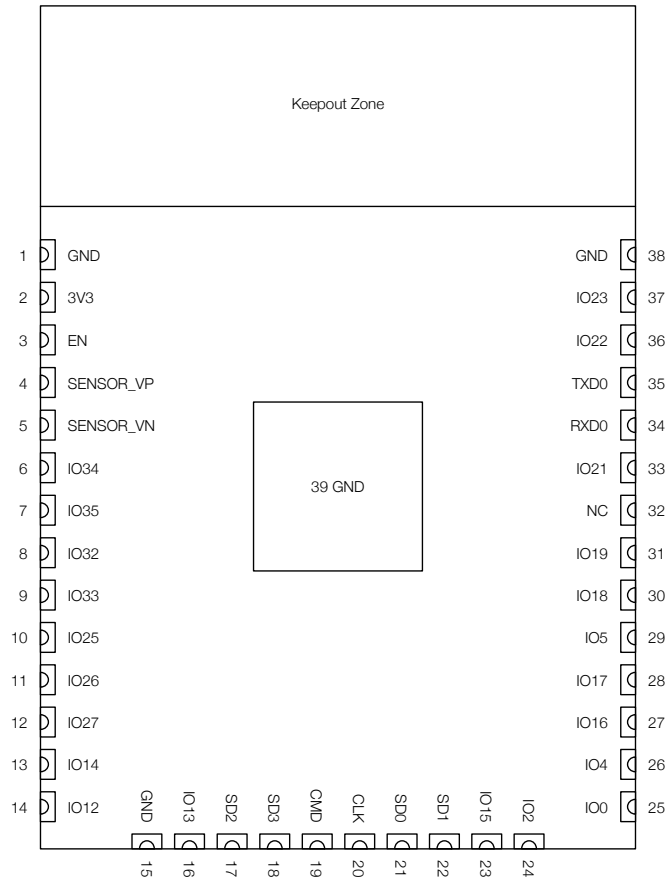


Figure 1: ESP32-WROOM-32 Pin Layout (Top View)

2.2 Pin Description

ESP32-WROOM-32 has 38 pins. See pin definitions in Table 2.

Table 2: Pin Definitions

| Name | No. | Type | Function |
|-----------|-----|------|--|
| GND | 1 | P | Ground |
| 3V3 | 2 | P | Power supply |
| EN | 3 | I | Module-enable signal. Active high. |
| SENSOR_VP | 4 | I | GPIO36, ADC1_CH0, RTC_GPIO0 |
| SENSOR_VN | 5 | I | GPIO39, ADC1_CH3, RTC_GPIO3 |
| IO34 | 6 | I | GPIO34, ADC1_CH6, RTC_GPIO4 |
| IO35 | 7 | I | GPIO35, ADC1_CH7, RTC_GPIO5 |
| IO32 | 8 | I/O | GPIO32, XTAL_32K_P (32.768 kHz crystal oscillator input), ADC1_CH4, TOUCH9, RTC_GPIO9 |
| IO33 | 9 | I/O | GPIO33, XTAL_32K_N (32.768 kHz crystal oscillator output), ADC1_CH5, TOUCH8, RTC_GPIO8 |

| Name | No. | Type | Function |
|----------|-----|------|--|
| IO25 | 10 | I/O | GPIO25, DAC_1, ADC2_CH8, RTC_GPIO6, EMAC_RXD0 |
| IO26 | 11 | I/O | GPIO26, DAC_2, ADC2_CH9, RTC_GPIO7, EMAC_RXD1 |
| IO27 | 12 | I/O | GPIO27, ADC2_CH7, TOUCH7, RTC_GPIO17, EMAC_RX_DV |
| IO14 | 13 | I/O | GPIO14, ADC2_CH6, TOUCH6, RTC_GPIO16, MTMS, HSPICLK, HS2_CLK, SD_CLK, EMAC_TXD2 |
| IO12 | 14 | I/O | GPIO12, ADC2_CH5, TOUCH5, RTC_GPIO15, MTDI, HSPIQ, HS2_DATA2, SD_DATA2, EMAC_TXD3 |
| GND | 15 | P | Ground |
| IO13 | 16 | I/O | GPIO13, ADC2_CH4, TOUCH4, RTC_GPIO14, MTCK, HSPID, HS2_DATA3, SD_DATA3, EMAC_RX_ER |
| SHD/SD2* | 17 | I/O | GPIO9, SD_DATA2, SPIHD, HS1_DATA2, U1RXD |
| SWP/SD3* | 18 | I/O | GPIO10, SD_DATA3, SPIWP, HS1_DATA3, U1TXD |
| SCS/CMD* | 19 | I/O | GPIO11, SD_CMD, SPICS0, HS1_CMD, U1RTS |
| SCK/CLK* | 20 | I/O | GPIO6, SD_CLK, SPICLK, HS1_CLK, U1CTS |
| SDO/SD0* | 21 | I/O | GPIO7, SD_DATA0, SPIQ, HS1_DATA0, U2RTS |
| SDI/SD1* | 22 | I/O | GPIO8, SD_DATA1, SPID, HS1_DATA1, U2CTS |
| IO15 | 23 | I/O | GPIO15, ADC2_CH3, TOUCH3, MTDO, HSPICS0, RTC_GPIO13, HS2_CMD, SD_CMD, EMAC_RXD3 |
| IO2 | 24 | I/O | GPIO2, ADC2_CH2, TOUCH2, RTC_GPIO12, HSPIWP, HS2_DATA0, SD_DATA0 |
| IO0 | 25 | I/O | GPIO0, ADC2_CH1, TOUCH1, RTC_GPIO11, CLK_OUT1, EMAC_TX_CLK |
| IO4 | 26 | I/O | GPIO4, ADC2_CH0, TOUCH0, RTC_GPIO10, HSPICLK, HS2_DATA1, SD_DATA1, EMAC_TX_ER |
| IO16 | 27 | I/O | GPIO16, HS1_DATA4, U2RXD, EMAC_CLK_OUT |
| IO17 | 28 | I/O | GPIO17, HS1_DATA5, U2TXD, EMAC_CLK_OUT_180 |
| IO5 | 29 | I/O | GPIO5, VSPICS0, HS1_DATA6, EMAC_RX_CLK |
| IO18 | 30 | I/O | GPIO18, VSPICLK, HS1_DATA7 |
| IO19 | 31 | I/O | GPIO19, VSPIQ, U0CTS, EMAC_TXD0 |
| NC | 32 | - | - |
| IO21 | 33 | I/O | GPIO21, VSPIHD, EMAC_TX_EN |
| RXD0 | 34 | I/O | GPIO3, U0RXD, CLK_OUT2 |
| TXD0 | 35 | I/O | GPIO1, U0TXD, CLK_OUT3, EMAC_RXD2 |
| IO22 | 36 | I/O | GPIO22, VSPIWP, U0RTS, EMAC_TXD1 |
| IO23 | 37 | I/O | GPIO23, VSPID, HS1_STROBE |
| GND | 38 | P | Ground |

Notice:

* Pins SCK/CLK, SDO/SD0, SDI/SD1, SHD/SD2, SWP/SD3 and SCS/CMD, namely, GPIO6 to GPIO11 are connected to the integrated SPI flash integrated on the module and are not recommended for other uses.

2.3 Strapping Pins

ESP32 has five strapping pins, which can be seen in Chapter 6 Schematics:

- MTDI
- GPIO0
- GPIO2
- MTDO
- GPIO5

Software can read the values of these five bits from register "GPIO_STRAPPING".

During the chip's system reset release (power-on-reset, RTC watchdog reset and brownout reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down. The strapping bits configure the device's boot mode, the operating voltage of VDD_SDIO and other initial system settings.

Each strapping pin is connected to its internal pull-up/pull-down during the chip reset. Consequently, if a strapping pin is unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of the strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32.

After reset release, the strapping pins work as normal-function pins.

Refer to Table 3 for a detailed boot-mode configuration by strapping pins.

Table 3: Strapping Pins

| Voltage of Internal LDO (VDD_SDIO) | | | | | |
|---|-----------|--|---|---|--|
| Pin | Default | 3.3 V | | 1.8 V | |
| MTDI | Pull-down | 0 | | 1 | |
| Bootling Mode | | | | | |
| Pin | Default | SPI Boot | | Download Boot | |
| GPIO0 | Pull-up | 1 | | 0 | |
| GPIO2 | Pull-down | Don't-care | | 0 | |
| Enabling/Disabling Debugging Log Print over U0TXD During Bootling | | | | | |
| Pin | Default | U0TXD Active | | U0TXD Silent | |
| MTDO | Pull-up | 1 | | 0 | |
| Timing of SDIO Slave | | | | | |
| Pin | Default | Falling-edge Sampling Falling-edge Output | Falling-edge Sampling Rising-edge Output | Rising-edge Sampling Falling-edge Output | Rising-edge Sampling Rising-edge Output |
| MTDO | Pull-up | 0 | 0 | 1 | 1 |
| GPIO5 | Pull-up | 0 | 1 | 0 | 1 |

Note:

- Firmware can configure register bits to change the settings of "Voltage of Internal LDO (VDD_SDIO)" and "Timing of SDIO Slave" after bootling.
- The module integrates a 3.3 V SPI flash, so the pin MTDI cannot be set to 1 when the module is powered up.

3. Functional Description

This chapter describes the modules and functions integrated in ESP32-WROOM-32.

3.1 CPU and Internal Memory

ESP32-D0WDQ6 contains two low-power Xtensa® 32-bit LX6 microprocessors. The internal memory includes:

- 448 KB of ROM for booting and core functions.
- 520 KB of on-chip SRAM for data and instructions.
- 8 KB of SRAM in RTC, which is called RTC FAST Memory and can be used for data storage; it is accessed by the main CPU during RTC Boot from the Deep-sleep mode.
- 8 KB of SRAM in RTC, which is called RTC SLOW Memory and can be accessed by the co-processor during the Deep-sleep mode.
- 1 Kbit of eFuse: 256 bits are used for the system (MAC address and chip configuration) and the remaining 768 bits are reserved for customer applications, including flash-encryption and chip-ID.

3.2 External Flash and SRAM

ESP32 supports multiple external QSPI flash and SRAM chips. More details can be found in Chapter SPI in the [ESP32 Technical Reference Manual](#). ESP32 also supports hardware encryption/decryption based on AES to protect developers' programs and data in flash.

ESP32 can access the external QSPI flash and SRAM through high-speed caches.

- The external flash can be mapped into CPU instruction memory space and read-only memory space simultaneously.
 - When external flash is mapped into CPU instruction memory space, up to 11 MB + 248 KB can be mapped at a time. Note that if more than 3 MB + 248 KB are mapped, cache performance will be reduced due to speculative reads by the CPU.
 - When external flash is mapped into read-only data memory space, up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads are supported.
- External SRAM can be mapped into CPU data memory space. Up to 4 MB can be mapped at a time. 8-bit, 16-bit and 32-bit reads and writes are supported.

ESP32-WROOM-32 integrates a 4 MB SPI flash, which is connected to GPIO6, GPIO7, GPIO8, GPIO9, GPIO10 and GPIO11. These six pins cannot be used as regular GPIOs.

3.3 Crystal Oscillators

The module uses a 40-MHz crystal oscillator.

3.4 RTC and Low-Power Management

With the use of advanced power-management technologies, ESP32 can switch between different power modes.

For details on ESP32's power consumption in different power modes, please refer to section "RTC and Low-Power Management" in [ESP32 Datasheet](#).

4. Peripherals and Sensors

Please refer to Section Peripherals and Sensors in [ESP32 Datasheet](#).

Note:

External connections can be made to any GPIO except for GPIOs in the range 6-11. These six GPIOs are connected to the module's integrated SPI flash. For details, please see Section 6 Schematics.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings listed in Table 4 below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device that should follow the [recommended operating conditions](#).

Table 4: Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Unit |
|----------------|------------------------------|------|-------|------|
| VDD33 | Power supply voltage | -0.3 | 3.6 | V |
| I_{output}^1 | Cumulative IO output current | - | 1,100 | mA |
| T_{store} | Storage temperature | -40 | 150 | °C |

1. The module worked properly after a 24-hour test in ambient temperature at 25 °C, and the IOs in three domains (VDD3P3_RTC, VDD3P3_CPU, VDD_SDIO) output high logic level to ground. Please note that pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.
2. Please see Appendix IO_MUX of [ESP32 Datasheet](#) for IO's power domain.

5.2 Recommended Operating Conditions

Table 5: Recommended Operating Conditions

| Symbol | Parameter | Min | Typical | Max | Unit |
|-----------|--|-----|---------|-----|------|
| VDD33 | Power supply voltage | 2.7 | 3.3 | 3.6 | V |
| I_{VDD} | Current delivered by external power supply | 0.5 | - | - | A |
| T | Operating temperature | -40 | - | 85 | °C |

5.3 DC Characteristics (3.3 V, 25 °C)

Table 6: DC Characteristics (3.3 V, 25 °C)

| Symbol | Parameter | | Min | Typ | Max | Unit |
|----------|---|---|---------------------|-----|---------------------|------|
| C_{IN} | Pin capacitance | | - | 2 | - | pF |
| V_{IH} | High-level input voltage | | $0.75 \times VDD^1$ | - | $VDD^1 + 0.3$ | V |
| V_{IL} | Low-level input voltage | | -0.3 | - | $0.25 \times VDD^1$ | V |
| I_{IH} | High-level input current | | - | - | 50 | nA |
| I_{IL} | Low-level input current | | - | - | 50 | nA |
| V_{OH} | High-level output voltage | | $0.8 \times VDD^1$ | - | - | V |
| V_{OL} | Low-level output voltage | | - | - | $0.1 \times VDD^1$ | V |
| I_{OH} | High-level source current ($VDD^1 = 3.3$ V, $V_{OH} \geq 2.64$ V, output drive strength set to the maximum) | VDD3P3_CPU power domain ^{1, 2} | - | 40 | - | mA |
| | | VDD3P3_RTC power domain ^{1, 2} | - | 40 | - | mA |
| | | VDD_SDIO power domain ^{1, 3} | - | 20 | - | mA |

| Symbol | Parameter | Min | Typ | Max | Unit |
|----------------|--|-----|-----|-----|-----------|
| I_{OL} | Low-level sink current ($V_{DD}^1 = 3.3\text{ V}$, $V_{OL} = 0.495\text{ V}$, output drive strength set to the maximum) | - | 28 | - | mA |
| R_{PU} | Resistance of internal pull-up resistor | - | 45 | - | $k\Omega$ |
| R_{PD} | Resistance of internal pull-down resistor | - | 45 | - | $k\Omega$ |
| V_{IL_nRST} | Low-level input voltage of CHIP_PU to power off the chip | - | - | 0.6 | V |

Notes:

1. Please see Appendix IO_MUX of [ESP32 Datasheet](#) for IO's power domain. VDD is the I/O voltage for a particular power domain of pins.
2. For VDD3P3_CPU and VDD3P3_RTC power domain, per-pin current sourced in the same domain is gradually reduced from around 40 mA to around 29 mA, $V_{OH} \geq 2.64\text{ V}$, as the number of current-source pins increases.
3. Pins occupied by flash and/or PSRAM in the VDD_SDIO power domain were excluded from the test.

5.4 Wi-Fi Radio

Table 7: Wi-Fi Radio Characteristics

| Parameter | Condition | Min | Typical | Max | Unit |
|----------------------------|-----------------|------|---------|------|----------|
| Input frequency | - | 2412 | - | 2484 | MHz |
| Output impedance* | - | - | * | - | Ω |
| TX power | 11n, MCS7 | 12 | 13 | 14 | dBm |
| | 11b mode | 17.5 | 18.5 | 20 | dBm |
| Sensitivity | 11b, 1 Mbps | - | -98 | - | dBm |
| | 11b, 11 Mbps | - | -89 | - | dBm |
| | 11g, 6 Mbps | - | -92 | - | dBm |
| | 11g, 54 Mbps | - | -74 | - | dBm |
| | 11n, HT20, MCS0 | - | -91 | - | dBm |
| | 11n, HT20, MCS7 | - | -71 | - | dBm |
| | 11n, HT40, MCS0 | - | -89 | - | dBm |
| | 11n, HT40, MCS7 | - | -69 | - | dBm |
| Adjacent channel rejection | 11g, 6 Mbps | - | 31 | - | dB |
| | 11g, 54 Mbps | - | 14 | - | dB |
| | 11n, HT20, MCS0 | - | 31 | - | dB |
| | 11n, HT20, MCS7 | - | 13 | - | dB |

*For the modules that use IPEX antennas, the output impedance is 50 Ω . For other modules without IPEX antennas, users do not need to concern about the output impedance.

5.5 BLE Radio

5.5.1 Receiver

Table 8: Receiver Characteristics – BLE

| Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------------|---------------------|-----|-----|-----|------|
| Sensitivity @30.8% PER | - | - | -97 | - | dBm |
| Maximum received signal @30.8% PER | - | 0 | - | - | dBm |
| Co-channel C/I | - | - | +10 | - | dB |
| Adjacent channel selectivity C/I | F = F0 + 1 MHz | - | -5 | - | dB |
| | F = F0 - 1 MHz | - | -5 | - | dB |
| | F = F0 + 2 MHz | - | -25 | - | dB |
| | F = F0 - 2 MHz | - | -35 | - | dB |
| | F = F0 + 3 MHz | - | -25 | - | dB |
| | F = F0 - 3 MHz | - | -45 | - | dB |
| Out-of-band blocking performance | 30 MHz ~ 2000 MHz | -10 | - | - | dBm |
| | 2000 MHz ~ 2400 MHz | -27 | - | - | dBm |
| | 2500 MHz ~ 3000 MHz | -27 | - | - | dBm |
| | 3000 MHz ~ 12.5 GHz | -10 | - | - | dBm |
| Intermodulation | - | -36 | - | - | dBm |

5.5.2 Transmitter

Table 9: Transmitter Characteristics – BLE

| Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------------------|------------------|-----|-------|-----|----------------|
| RF transmit power | - | - | 0 | - | dBm |
| Gain control step | - | - | 3 | - | dBm |
| RF power control range | - | -12 | - | +9 | dBm |
| Adjacent channel transmit power | F = F0 ± 2 MHz | - | -52 | - | dBm |
| | F = F0 ± 3 MHz | - | -58 | - | dBm |
| | F = F0 ± > 3 MHz | - | -60 | - | dBm |
| Δf_{1avg} | - | - | - | 265 | kHz |
| Δf_{2max} | - | 247 | - | - | kHz |
| $\Delta f_{2avg}/\Delta f_{1avg}$ | - | - | -0.92 | - | - |
| ICFT | - | - | -10 | - | kHz |
| Drift rate | - | - | 0.7 | - | kHz/50 μ s |
| Drift | - | - | 2 | - | kHz |

5.6 Reflow Profile

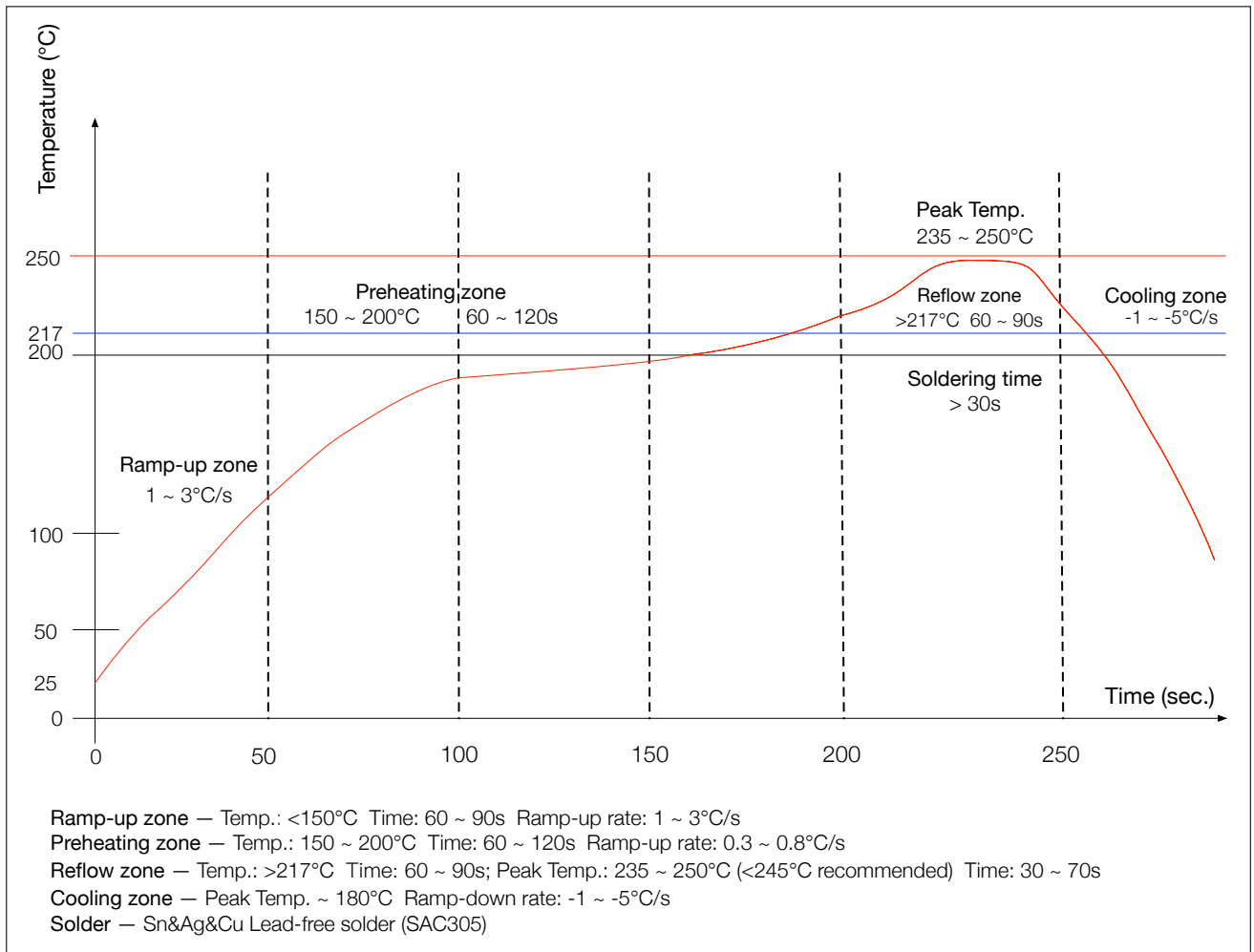


Figure 2: Reflow Profile

6. Schematics

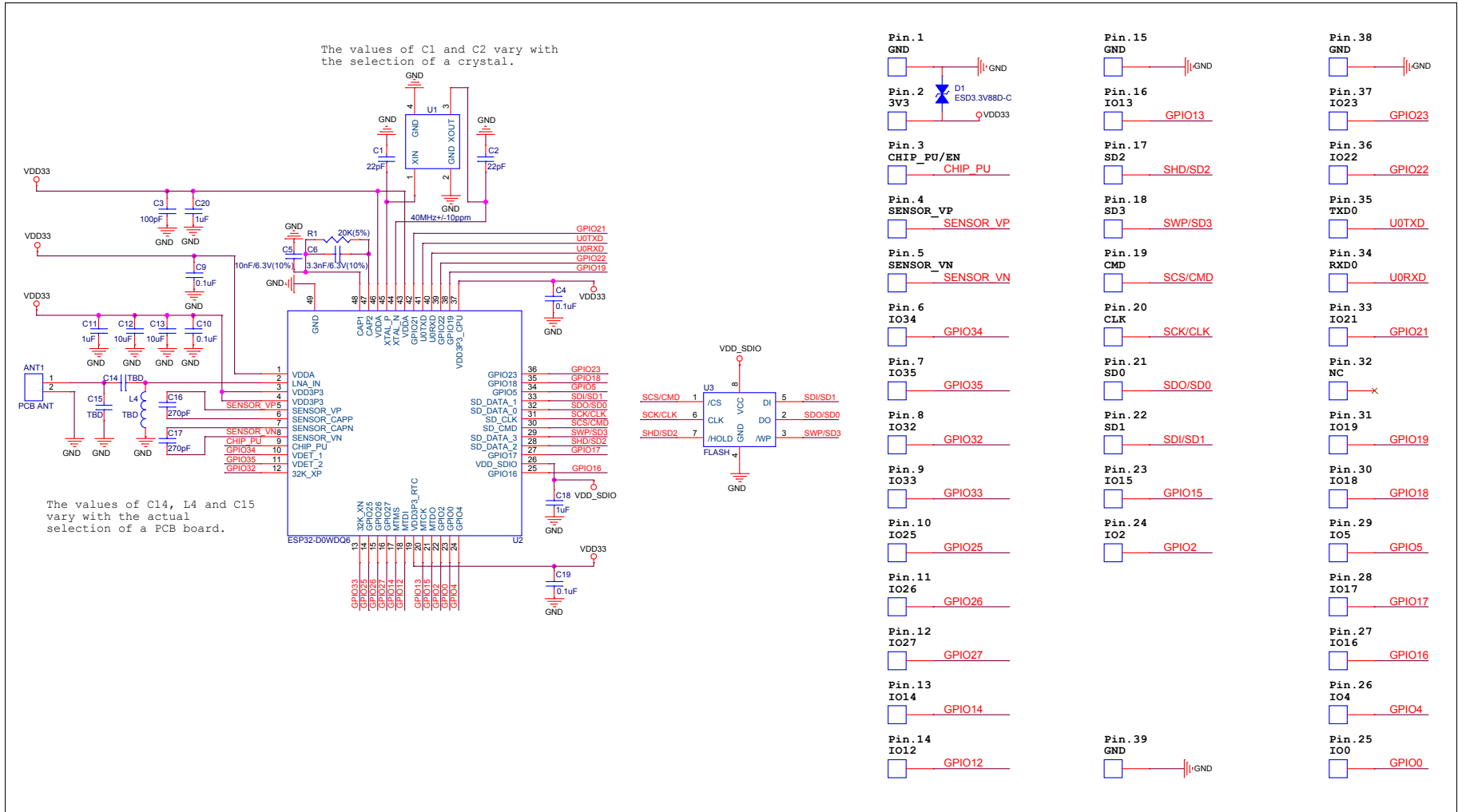


Figure 3: ESP32-WROOM-32 Schematics

7. Peripheral Schematics

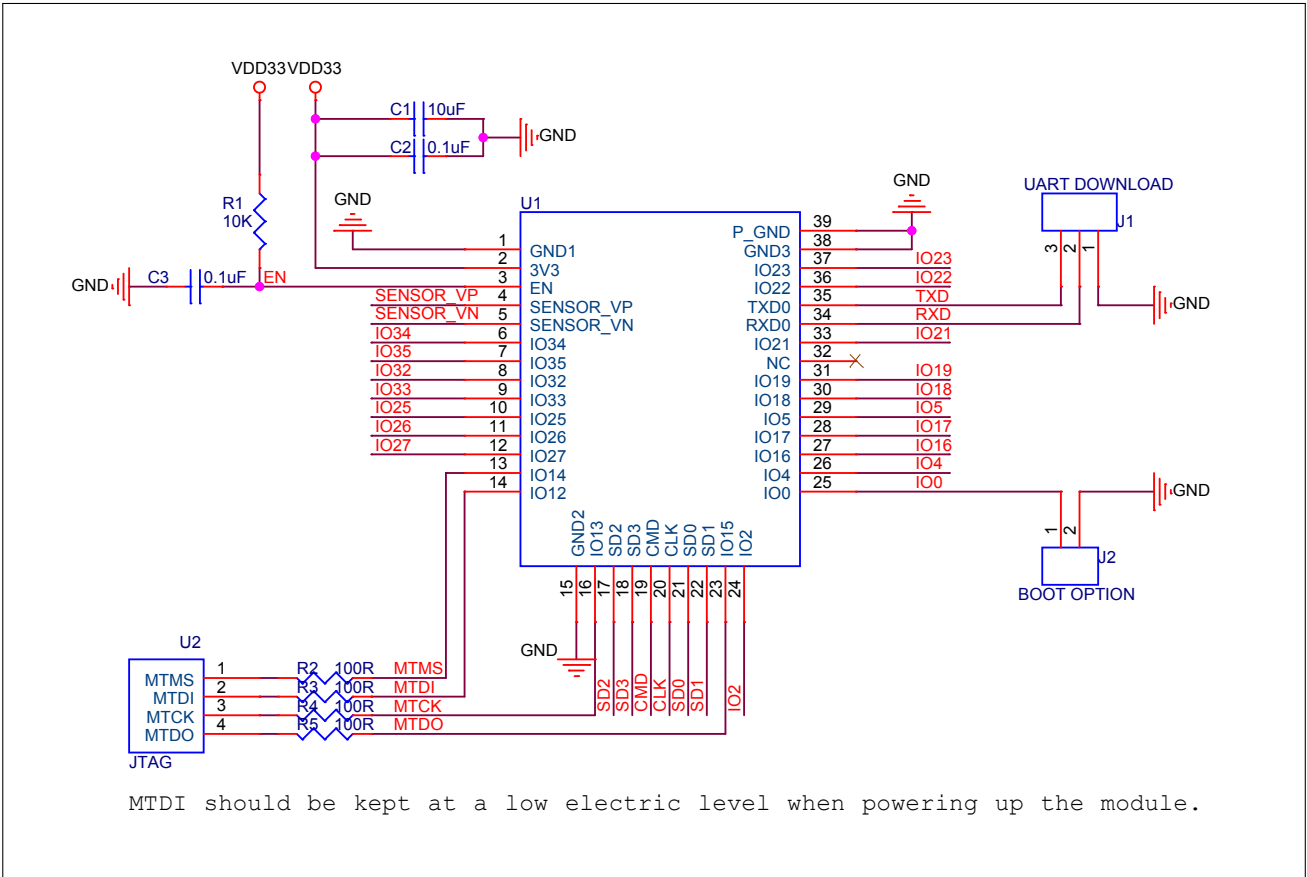


Figure 4: ESP32-WROOM-32 Peripheral Schematics

Note:

Soldering Pad 39 to the Ground of the base board is not necessary for a satisfactory thermal performance. If users do want to solder it, they need to ensure that the correct quantity of soldering paste is applied.

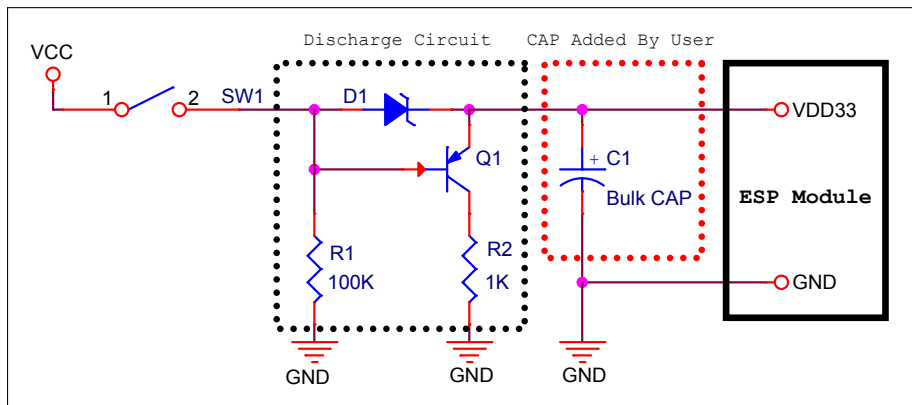
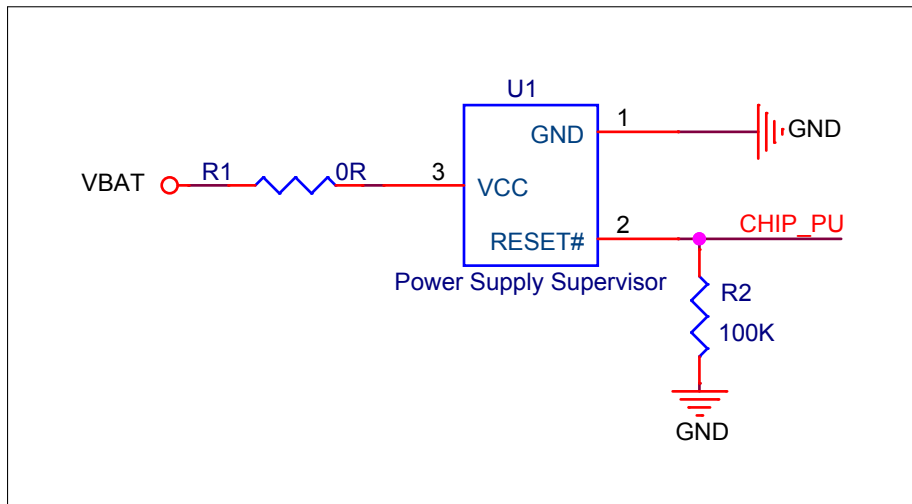


Figure 5: Discharge Circuit for VDD33 Rail

Note:

The discharge circuit can be applied in scenarios where ESP32 is powered on and off repeatedly by switching the power rails, and there is a large capacitor on the VDD33 rail. For details, please refer to Section **Power Scheme** in [ESP32 Datasheet](#).

**Figure 6: Reset Circuit****Note:**

When battery is used as the power supply for ESP32 series of chips and modules, a supply voltage supervisor is recommended to avoid boot failure due to low voltage. Users are recommended to pull CHIP_PU low if the power supply for ESP32 is below 2.3 V.

8. Physical Dimensions

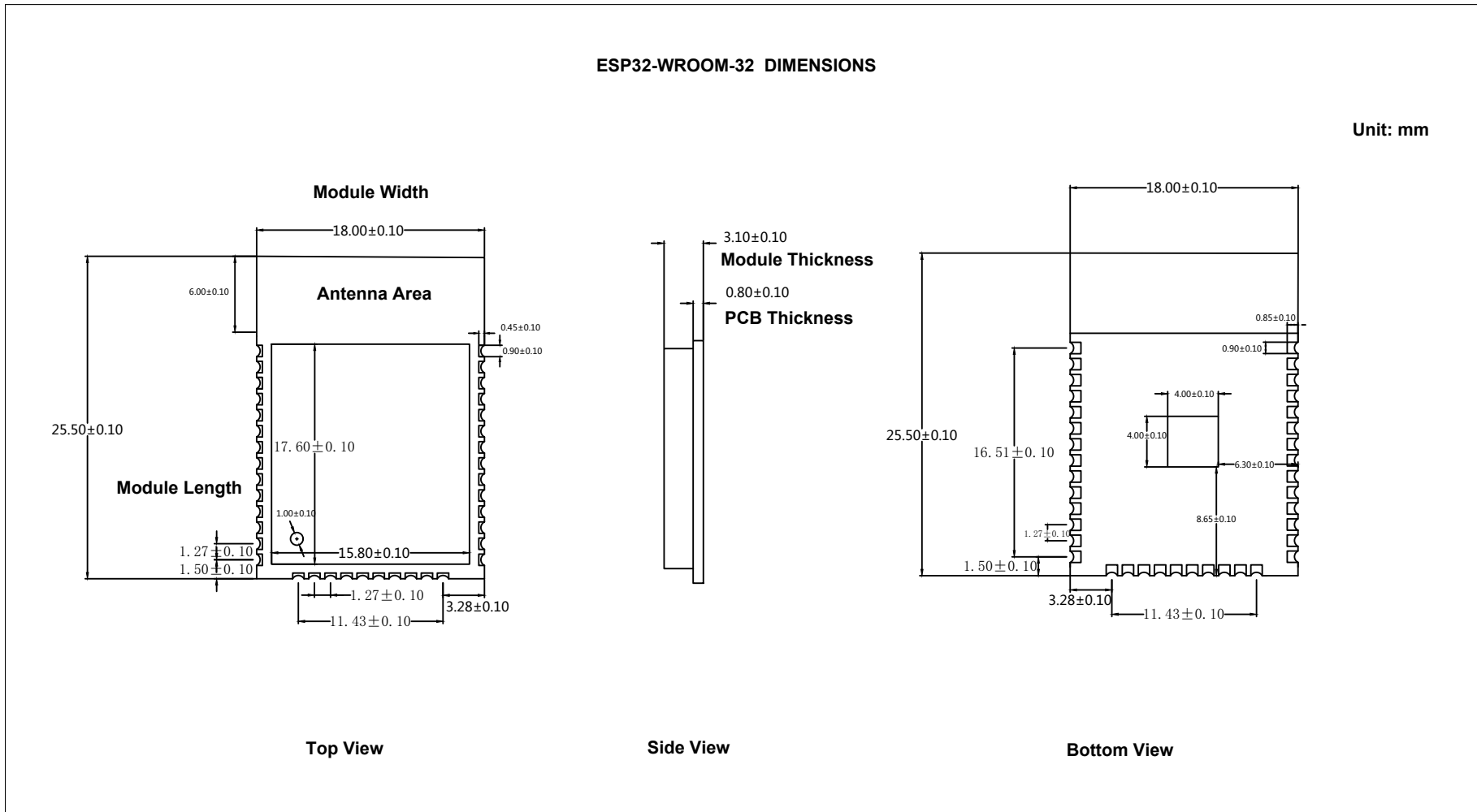


Figure 7: Physical Dimensions of ESP32-WROOM-32

9. Recommended PCB Land Pattern

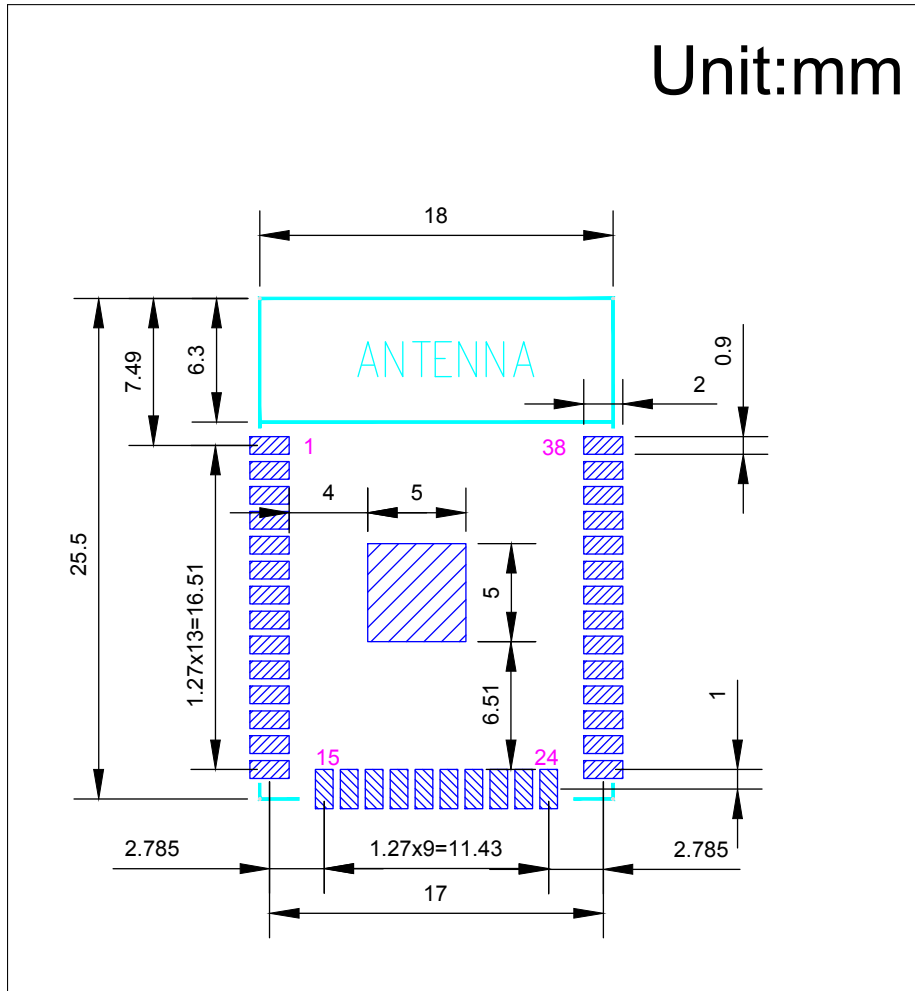


Figure 8: Recommended PCB Land Pattern

10. Learning Resources

10.1 Must-Read Documents

The following link provides documents related to ESP32.

- [ESP32 Datasheet](#)
This document provides an introduction to the specifications of the ESP32 hardware, including overview, pin definitions, functional description, peripheral interface, electrical characteristics, etc.
- [ESP-IDF Programming Guide](#)
It hosts extensive documentation for ESP-IDF ranging from hardware guides to API reference.
- [ESP32 Technical Reference Manual](#)
The manual provides detailed information on how to use the ESP32 memory and peripherals.
- [ESP32 Hardware Resources](#)
The zip files include the schematics, PCB layout, Gerber and BOM list of ESP32 modules and development boards.
- [ESP32 Hardware Design Guidelines](#)
The guidelines outline recommended design practices when developing standalone or add-on systems based on the ESP32 series of products, including the ESP32 chip, the ESP32 modules and development boards.
- [ESP32 AT Instruction Set and Examples](#)
This document introduces the ESP32 AT commands, explains how to use them, and provides examples of several common AT commands.
- [Espressif Products Ordering Information](#)

10.2 Must-Have Resources

Here are the ESP32-related must-have resources.

- [ESP32 BBS](#)
This is an Engineer-to-Engineer (E2E) Community for ESP32 where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
- [ESP32 GitHub](#)
ESP32 development projects are freely distributed under Espressif's MIT license on GitHub. It is established to help developers get started with ESP32 and foster innovation and the growth of general knowledge about the hardware and software surrounding ESP32 devices.
- [ESP32 Tools](#)
This is a webpage where users can download ESP32 Flash Download Tools and the zip file "ESP32 Certification and Test".
- [ESP-IDF](#)
This webpage links users to the official IoT development framework for ESP32.
- [ESP32 Resources](#)
This webpage provides the links to all available ESP32 documents, SDK and tools.

Revision History

| Date | Version | Release notes |
|---------|---------|--|
| 2019.01 | V2.8 | Changed the RF power control range in Table 9 from $-12 \sim +12$ to $-12 \sim +9$ dBm. |
| 2018.10 | V2.7 | Added "Cumulative IO output current" entry to Table 4: Absolute Maximum Ratings; Added more parameters to Table 6: DC Characteristics. |
| 2018.08 | V2.6 | <ul style="list-style-type: none"> Added reliability test items the module has passed in Table 1: ESP32-WROOM-32 Specifications, and removed software-specific information; Updated section 3.4: RTC and Low-Power Management; Changed the module's dimensions from (18 ± 0.2) mm x (25.5 ± 0.2) mm x (3.1 ± 0.15) mm to (18.00 ± 0.10) mm x (25.50 ± 0.10) mm x (3.10 ± 0.10) mm; Updated Figure 8: Physical Dimensions; Updated Table 7: Wi-Fi Radio. |
| 2018.06 | V2.5 | <ul style="list-style-type: none"> Changed the module name to ESP32-WROOM-32; Deleted Temperature Sensor in Table 1: ESP32-WROOM-32 Specifications; Updated Chapter 3: Functional Description; Added Chapter 8: Recommended PCB Land Pattern; Changes to electrical characteristics: <ul style="list-style-type: none"> Updated Table 4: Absolute Maximum Ratings; Added Table 5: Recommended Operating Conditions; Added Table 6: DC Characteristics; Updated the values of "Gain control step", "Adjacent channel transmit power" in Table 9: Transmitter Characteristics - BLE. |
| 2018.03 | V2.4 | Updated Table 1 in Chapter 1. |
| 2018.01 | V2.3 | Deleted information on LNA pre-amplifier; Updated section 3.4 RTC and Low-Power Management; Added reset circuit in Chapter 7 and a note to it. |
| 2017.10 | V2.2 | Updated the description of the chip's system reset in Section 2.3 Strapping Pins; Deleted "Association sleep pattern" in Table "Power Consumption by Power Modes" and added notes to Active sleep and Modem-sleep; Updated the note to Figure 4 Peripheral Schematics; Added discharge circuit for VDD33 rail in Chapter 7 and a note to it. |
| 2017.09 | V2.1 | Updated operating voltage/power supply range updated to $2.7 \sim 3.6$ V; Updated Chapter 7. |
| 2017.08 | V2.0 | Changed the sensitivity of NZIF receiver to -97 dBm in Table 1; Updated the dimensions of the module; Updated Table "Power Consumption by Power Modes" Power Consumption by Power Modes, and added two notes to it; Updated Table 4, 7, 8, 9; Added Chapter 8; Added the link to certification download . |
| 2017.06 | V1.9 | Added a note to Section 2.1 Pin Layout; Updated Section 3.3 Crystal Oscillators; Updated Figure 3 ESP-WROOM-32 Schematics; |

| Date | Version | Release notes |
|---------|---------|---|
| | | Added Documentation Change Notification. |
| 2017.05 | V1.8 | Updated Figure 1 Top and Side View of ESP32-WROOM-32 (ESP-WROOM-32). |
| 2017.04 | V1.7 | Added the module's dimensional tolerance; Changed the input impedance value of 50Ω in Table 7 Wi-Fi Radio Characteristics to output impedance value of $30+j10\Omega$. |
| 2017.04 | V1.6 | Added Figure 2 Reflow Profile. |
| 2017.03 | V1.5 | Updated Section 2.2 Pin Description; Updated Section 3.2 External Flash and SRAM; Updated Section 4 Peripherals and Sensors Description. |
| 2017.03 | V1.4 | Updated Chapter 1 Preface; Updated Chapter 2 Pin Definitions; Updated Chapter 3 Functional Description; Updated Table Recommended Operating Conditions; Updated Table 7 Wi-Fi Radio Characteristics; Updated Section 5.6 Reflow Profile; Added Chapter 10 Learning Resources. |
| 2016.12 | V1.3 | Updated Section 2.1 Pin Layout. |
| 2016.11 | V1.2 | Added Figure 7 Peripheral Schematics. |
| 2016.11 | V1.1 | Updated Chapter 6 Schematics. |
| 2016.08 | V1.0 | First release. |