安信可科技
Ai-Thinker

# Hi-12F-Kit Specification

Version V1.1.0

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# Document resume

| Version | Date | Develop/revise content | Edition | Approve |
|---------|------|------------------------|---------|---------|
| V1.1.0 | 2021.10.25 | First Edition | Xiaochen Li | Hong Xu |
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# Content

# 1. Product Overview

Hi-12F-Kit is a Wi-Fi development board developed by Shenzhen Ai-Thinker Technology Co., Ltd. It can be widely used in the development of WiFi related Internet of Things intelligent terminal products such as smart home, intelligent security and smart city.

The Hi-12F-Kit comes with the Hi-12F module, which uses the Hi3861V100 core processor chip. The chip is a highly integrated 2.4GHz low power SoC WiFi chip integrating IEEE 802.11b/g/n base-band and RF circuit including power amplifier P A, low noise amplifier LNA, RF balun, antenna switch and power management,etc; supports 20MHz standard bandwidth and 5MHz/10MHz narrow bandwidth for maximum 72.2Mbit/s physical layer rate. The chip WiFi baseband supports orthogonal frequency division multiplexing (OFDM) technology and is downward compatible with Direct Sequence Amplification (DSSS) and complementary code keying (CCK) technologies supporting various data rates for IEEE 802.11 b/g/n protocols.

The Hi-12F module on the Hi-12F-Kit uses Hi3861V100 chips that also integrate high-performance 32bit microprocessor, hardware security engine and rich peripheral interfaces including SPI, UART, I2C, PWM, GPIO and multiplexed ADC, high-speed SDIO2.0 Slave interface up to 50MHz; inside chip with SRAM and Flash, can operate independently and support programs on Flash.

The Hi-12F module supports Huawei LiteOS and third-party components, along with an open, easy-to-use development and commissioning operating environment.
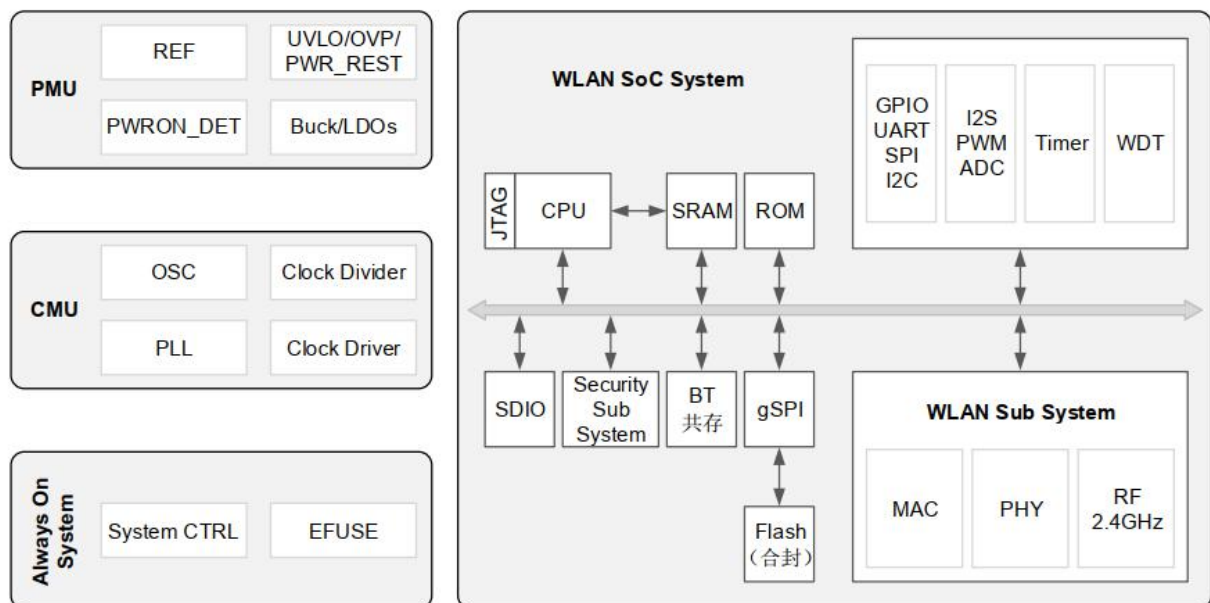


**Figure 1 Main chip architecture diagram**

## 1.1. Characteristic

- 1×1 2.4GHz frequency band (ch1~ch14)

- Support IEEE802.11b/g/n single antenna all data rate

- Supported by the maximum rate: 72.2Mbps@HT20 MCS7

- support STBC

- Support Short-GI

- Support STA and AP forms, maximum 6 STA access is supported as an AP.

- Support for WFA WPA/WPA2 personal, WPS2.0

- High-performance 32bit microprocessor with a maximum operating frequency of 160MHz

- Built in 352KB SRAM, 288KB ROM, embedded 2MB Flash

- Internal integrated EFUSE, supports secure storage, secure start up, and hardware ID

- Support for 256-node Mesh networking

- Support for AT commands, you can quickly start

- Open OS Huawei LiteOS, provides an open, efficient, and secure system development, operating environment

- The modules were packaged in SMD-22

- Support UART/SPI/I2C/GPIO/ADC/PWM/I2S/SDIO interface

## 2. Main parameters

**Table 1 Description of the main parameters**

| | |
|---|---|
| **Development board model** | Hi-12F-Kit |
| **Suitable module** | Hi-12F |
| **Package** | SMD-22 |
| **Size** | 25.40*48.26(±0.2)mm |
| **Antenna** | On-board PCB antenna |
| **Frequency range** | 2400 ~ 2483.5MHz |
| **Operating temperature** | -40 ℃ ~ 85 ℃ |
| **Storage environmen** | -40 ℃ ~ 125 ℃ , < 90%RH |
| **Power supply range** | Voltage: 5V, Electrical current ≥ 500mA |
| **Support Interface** | UART/SPI/I2C/GPIO/ADC/PWM /I2S/SDIO |
| **IO** | 16 IO, including TX0\RX0 TX1\RX1 |
| **UART Rate** | Default 115200 |
| **Security** | WFA WPA/WPA2 personal　WPS2.0 |
| **Flash** | 2MB Flash |
| **WIFI** | 802.11b/g/n |

### 2.1. Power selection

You can supply Hi-12F-Kit in one of two ways as below:

■ Micro-USB interface power supply (default)

■ 3V3 with GND or 5V with GND pin supply

It is recommended to choose the first power supply mode: the Micro-USB interface power supply.

### 2.2. Static electricity requirements

The Hi-12F-Kit development board is an electrostatic sensitive device, and special precautions must be taken when handling it.

**Figure 2 ESD anti-static diagram**

## 2.3. Electrical characteristics

**Table 2 Electrical characteristics table**

| Parameters | | Conditions | Min | Typical Values | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage Micro-USB | | VCC | 4.5 | 5 | 5.3 | V |
| **Supply voltage** pin header | | VCC | 3.0 | 3.3 | 3.6 | V |
| I/O | Voltage | VDDIO1/ VDDIO2 | 3.125 | 3.3 | 3.6 | V |
| | VIH | - | 2.4 | - | 3.63 | V |
| | VIL | - | -0.3 | - | 0.8 | V |
| | VOH | - | 2.4 | - | - | V |
| | VOL | - | - | - | 0.4 | V |

## 2.4. WiFi RF performance

**Table 3 WiFi RF performance table**

| Description | Typical values | Unit |
|---|---|---|
| Working frequency | 2400 - 2483.5 | MHz |
| **Output power** | | |
| 11n mode HT20    PA output power | $14\pm2$ | dBm |
| 11g mode    PA output power | $15\pm2$ | dBm |
| 11b mode    PA output power | $17\pm2$ | dBm |
| **Receiving sensitivity** | | |

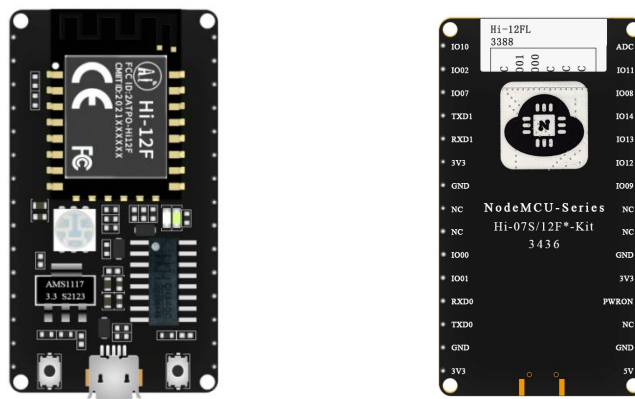| 11b, 1 Mbps | ≤-96 | dBm |
|---|---|---|
| 11b, 11 Mbps | ≤-89 | dBm |
| 6 Mbps (1/2 BPSK) | ≤-92 | dBm |
| 54 Mbps (3/4 64-QAM) | ≤-74 | dBm |
| HT20 (MCS7) | ≤-72 | dBm |

# 3. Appearance dimensions



**Figure 3 Appearance diagram of the development board (pictures and cover printing are for reference only, subject to physical objects)**
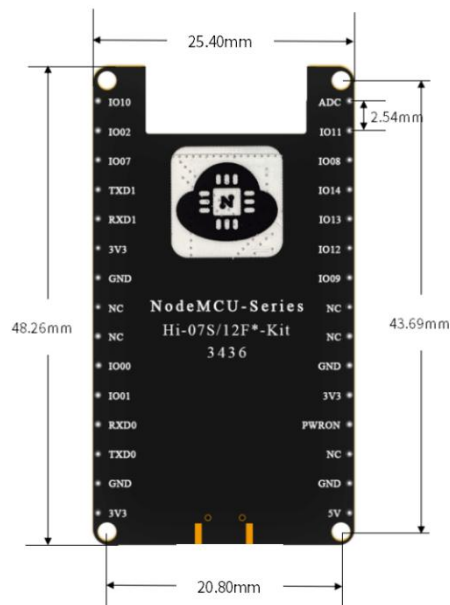


**Figure 4 Development board size diagram**
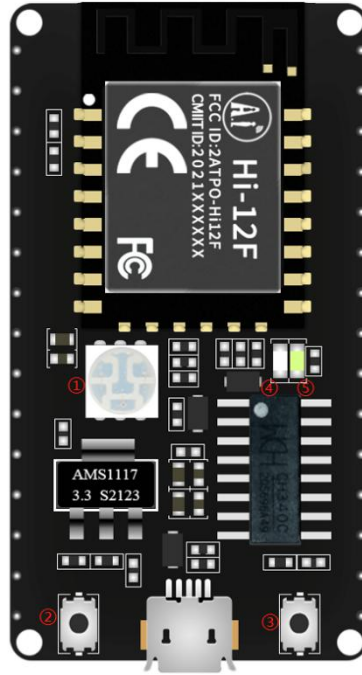
# 4. Indicator and button description



**Figure 5 Hi-12F-Kit indicator lamp and button location**

**Table 4 Hi-12F-Kitindicator lamp and button location**

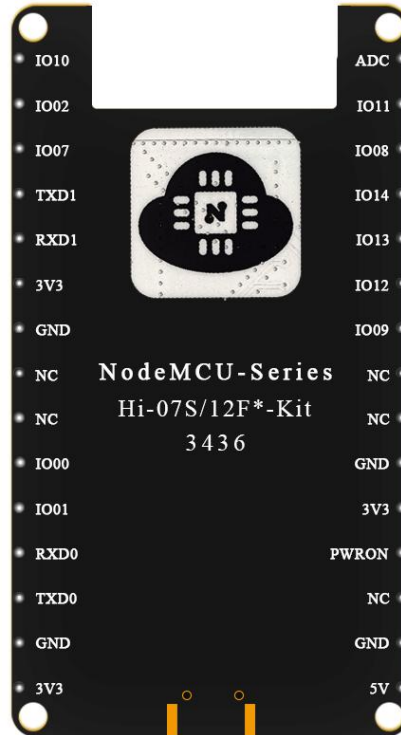| | |
|---|---|
| ① | IPEX |
| ② | RGB lamp    corresponding to IO12    IO13    IO09 |
| ③ | Reset key    corresponding to IO08 |
| ④ | Button KEY2    corresponding to IO07 |
| ⑤ | Warm light    corresponding to IO2 |

# 5. Pin definition



**Figure 6 Schematic diagram of development board pins (bottom view)**

Hi-12F-Kit has a total of 30 interfaces. As shown in the above pin diagram, the pin function definition table is the interface definition.

**Table 5 Pin function definition table**

| No. | Name | Function |
|-----|------|----------|
| 1 | IO10 | GPIO_00   UART1_TXD   SPI1_CLK   PWM3_OUT   I2C1_SDA   JTAG_TDO   HW_ID0 |
| 2 | IO02 | GPIO_02   UART1_RTS   SPI1_TXD   PWM2_OUT   JTAG_TRSTN   REFCLK_FREQ_STATUS |
| 3 | IO07 | GPIO_07   UART1_CTS   SPI0_RXD   ADC3   PWM0_OUT   I2S0_CLK   BT_ACTIVE   HW_ID5 |
| 4 | TXD1 | GPIO_06   UART1_TXD   SPI0_CLK   PWM3_OUT   I2S0_TX   COEX_SWITCH   JTAG_MODE |
| 5 | RXD1 | GPIO_05   UART1_RXD   SPI0_CS1   ADC2 |

| | | |
|---|---|---|
| | | PWM2_OUT   I2S0_MCK   BT_STATUS   HW_ID4 |
| 6 | 3V3 | Power supply, recommended for 3.3V, greater than 500mA |
| 7 | GND | Ground |
| 8 | NC | NC |
| 9 | NC | NC |
| 10 | IO00 | GPIO_00   UART1_TXD   SPI1_CLK   PWM3_OUT   I2C1_SDA   JTAG_TDO   HW_ID0 |
| 11 | IO01 | GPIO_01   GPIO_01   UART1_RXD   SPI1_RXD   PWM4_OUT   I2C1_SCL   BT_FREQ   JTAG_TCK   HW_ID1 |
| 12 | RXD0 | GPIO_04   UART0_LOG_RXD   ADC1   PWM1_OUT   I2C1_SCL   JTAG_TMS   HW_ID3 |
| 13 | TXD0 | GPIO_03   UART0_LOG_TXD   UART1_CTS   SPI1_CS1   PWM5_OUT   I2C1_SDA   JTAG_TDI |
| 14 | GND | Ground |
| 15 | 3V3 | Power supply, recommended for 3.3V, greater than 500mA |
| 16 | 5V | Power supply, 5V, greater than 500mA |
| 17 | GMD | Ground |
| 18 | NC | NC |
| 19 | PWRON | Chip PMU power on the enable pin    module is pulled up inside<br><br>0    power off<br><br>1    power on |
| 20 | 3V3 | Power supply, recommended for 3.3V, greater than 500mA |
| 21 | GND | GND |
| 22 | NC | NC |
| 23 | NC | NC |
| 24 | IO09 | GPIO_09   UART2_RTS   SPI0_TXD   SDIO_D2   ADC4   PWM0_OUT   I2S0_MCK   I2C0_SCL |

| 25 | IO12 | GPIO_12  UART2_RXD  SPI0_CS1  SDIO_CLK  ADC0  PWM3_OUT  I2S0_CLK  HW_ID7 |
|----|------|---------------------------------------------------------------------------|
| 26 | IO13 | GPIO_13  UART0_LOG_TXD  UART2_RTS  SDIO_D0  ADC6  PWM4_OUT  I2S0_WS  I2C0_SDA |
| 27 | IO14 | GPIO_14  UART0_LOG_RXD  UART2_CTS  SDIO_D1  PWM5_OUT  I2C0_SCL  HW_ID2 |
| 28 | IO08 | GPIO_08,UART1_RTS,SPI0_TXD,PWM1_OUT,I2S0_WS,WLAN_ACTIVE,JTAG_ENABLE |
| 29 | IO11 | GPIO_11  UART2_TXD  SPI0_RXD  SDIO_CMD  ADC5  PWM2_OUT  I2S0_RX  HW_ID6 |
| 30 | ADC | GPIO_11  UART2_TXD  SPI0_RXD  SDIO_CMD  ADC5  PWM2_OUT  I2S0_RX  HW_ID6 |

**Table 6 Module start up mode description table**

| Pin | Default status | Low level | High level |
|-----|---------------|-----------|-----------|
| IO2/REFCLK_FREQ_STATUS | pull down | 40MHz（default） | 24MHz |
| IO6/JTAG_MODE | pull down | Normal Function Mode (Default) | DFT test pattern |
| IO8/JTAG_ENABLE | pull down | General IO (Default) | JTAG enable |

Note: IO2/IO6/IO8 is a hardware configuration word and cannot be at high level when charged, otherwise the module cannot enter the normal operation state.
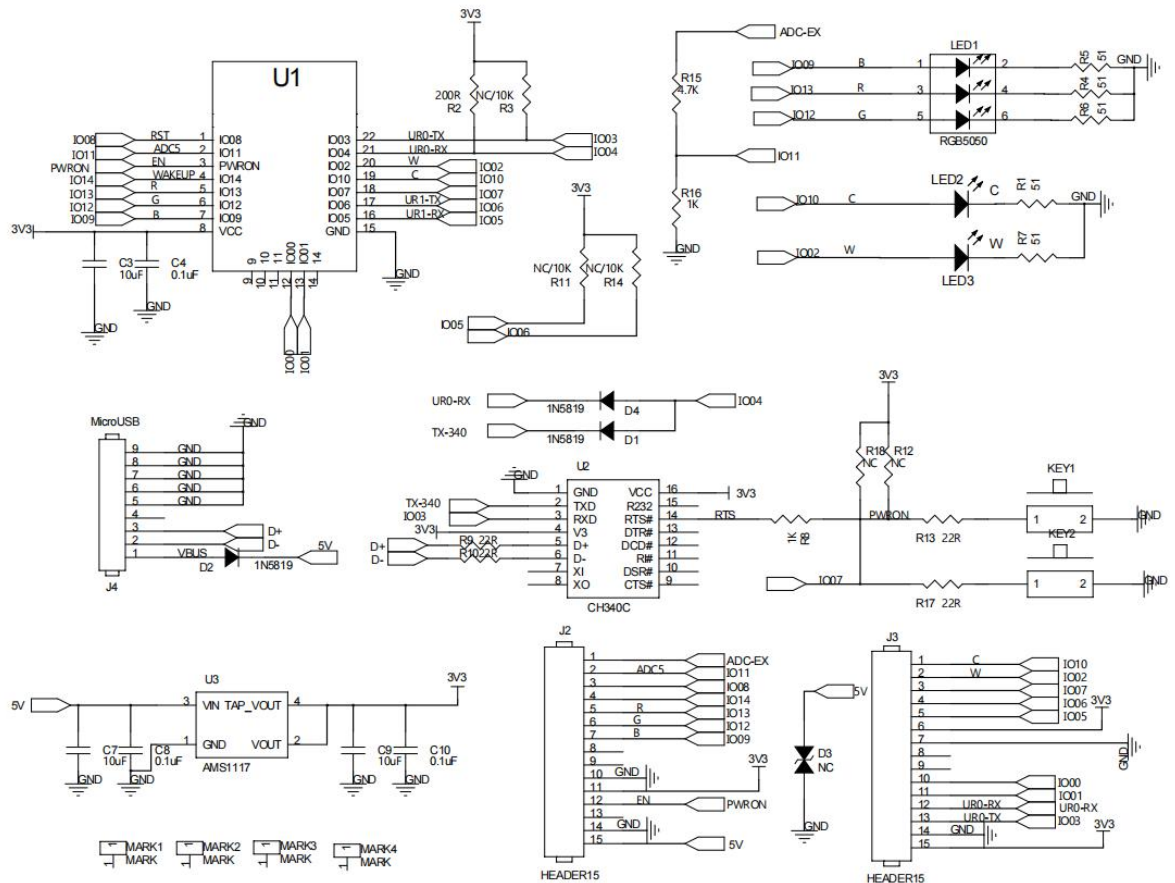
# 6. Schematic



**Figure 7 Schematic diagram of the development board**

# 7. Product related models

**Table 7 Product related model list**

| Model name | Power supply | Pin header TX1 and RX1 | Package | Size | Note |
|---|---|---|---|---|---|
| Hi-12F module | 3.3V I>500mA | / | SMD-22 | 24.0*16.0*3.2(±0.2)MM | |
| Hi-12FL module | 3.3V I>500mA | / | SMD-22 | 24.0*16.0*3.2(±0.2)MM | |
| Hi-07S module | 3.3V I>500mA | / | SMD-22 | 17.0*16.0*3.2(±0.2)MM | |
| Hi-07SL module | 3.3V I>500mA | / | SMD-22 | 17.0*16.0*3.2(±0.2)MM | |
| Hi-12F-Kit_V1.1.0 Development board | 5V, I>500mA | Support | DIP-30 | 25.40*48.26(±0.2)mm | |
| Hi-12FL-Kit_V1.1.0 Development board | 5V, I>500mA | Support | DIP-30 | 25.40*48.26(±0.2)mm | |
| Hi-07S-Kit_V1.1.0 Development board | 5V, I>500mA | Support | DIP-30 | 25.40*48.26(±0.2)mm | |
| Hi-07SL-Kit_V1.1.0 Development board | 5V, I>500mA | Support | DIP-30 | 25.40*48.26(±0.2)mm | |
| Product-related information    https://docs.ai-thinker.com/Hi3861 | | | | | |

# 8. Product packaging information

**Table 8 Packaging Information**

| Packing list | Modes of Packing | Quantity per pack (Electrostatic bag) | Quantity per pack (sealed bag |
|:---:|:---:|:---:|:---:|
| Hi-12F-Kit | Bubble cotton + electrostatic bag | 1pcs | 20pcs |

# 9. Contact us

Official website    https://www.ai-thinker.com

Development DOCS    https://docs.ai-thinker.com

Official Forum    http://bbs.ai-thinker.com

Sample purchase    https://aithinker.tmall.com

　　　　　　https://anxinke.taobao.com

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