ESP-12K SPECIFICATION

Version V1.0

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Formulation / Revision / Abolition of CV

Version	Date	Formulation / Revision	Make	Verify
V1.0	2020.04.10	First formulated	Yiji Xie	

CONTENT

1.PRODUCT DESCRIPTION.....V
2.ELECTRICAL PARAMETER.....IX
3.DIMENSION.....XI
4.PIN DEFINITION.....XIII
5.SCHEMATIC DIAGRAM.....XVI
6.DESIGN GUIDE.....XVII
7.RRFLOW SOLDERING CURER.....XX
8.PACKAGING.....XXI
9.CONTACT US.....XXI

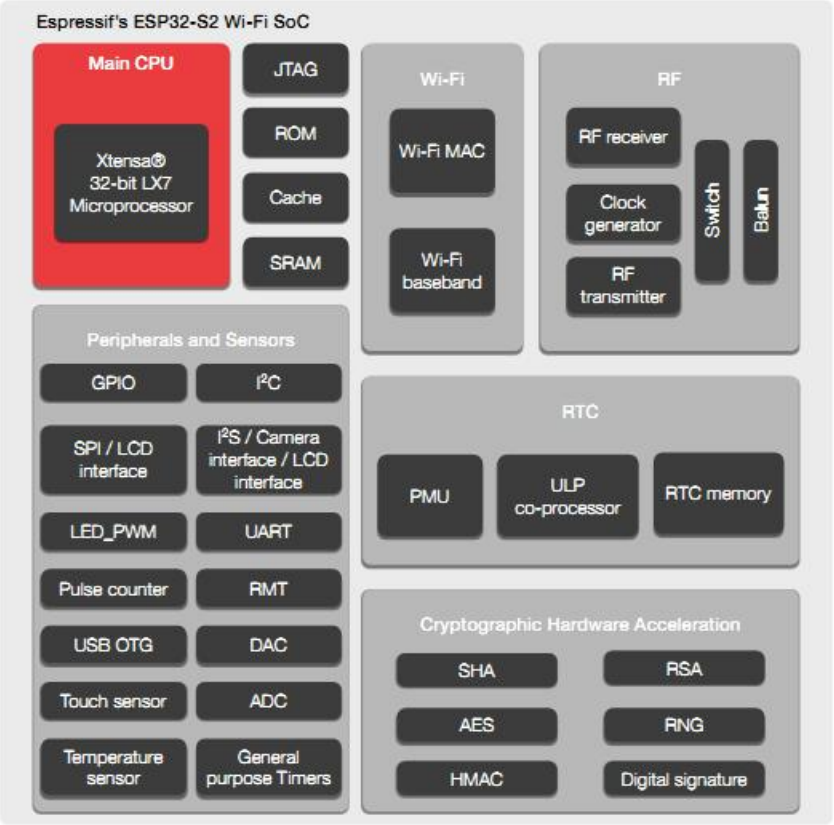
1.PRODUCT DESCRIPTION

ESP-12K is a Wi-Fi module developed by Ensink Technology. The core processor ESP32-S2 of this module is a highly integrated low-power Wi-Fi system-on-chip (SoC) designed for the Internet of Things (IoT) , Mobile devices, wearable electronic devices, smart home and other applications. ESP32-S2 has industry-leading low-power performance and RF performance, supports IEEE802.11b / g / n protocol, integrates Wi-Fi MAC, Wi-Fi RF and baseband, RF switch, RF Balun, power amplifier, low noise Amplifier, etc.

The ESP32-S2 chip is equipped with Xtensa® 32-bit LX7 single-core processor, and its operating frequency is up to 240 MHz. The chip supports secondary development without the use of other microcontrollers or processors. The chip has 320 KB SRAM and 128 KB ROM, and can be connected to flash and RAM through SPI / QSPI / OSPI and other interfaces. ESP32-S2 supports a variety of low-power operating states to meet the power consumption requirements of various application scenarios. The unique fine clock gating function, dynamic voltage clock frequency adjustment function, and RF output power adjustable function of the chip can achieve the best balance between communication distance, communication rate and power consumption.

ESP32-S2 provides a wealth of peripheral interfaces, including SPI, I2S, UART, I2C, LED PWM, LCD interface, Camera interface, ADC, DAC, touch sensor, temperature sensor and up to 43 GPIO.It supports the expansion of PSRAM on the periphery of the chip, and the ESP-12K module can be equipped with PSRAM. In addition, it includes a full-speed USB On-The-Go (OTG) interface that can support the use of USB communication.

ESP32-S2 has a variety of unique hardware security mechanisms. The hardware encryption accelerator supports AES, SHA, and RSA algorithms. The RNG, HMAC and Digital Signature (Digital Signature) modules provide more security features. Other security features include flash encryption and secure boot (se-cure boot) signature verification. The perfect security mechanism enables the chip to be perfectly applied to various encryption products.



Features

- Complete 802.11b / g / n Wi-Fi SoC module, data rate up to 150Mbps
- Built-in ESP32-S2 chip, Xtensa® single-core 32-bit LX7 microprocessor, support up to 240 MHz clock frequency, with 128KB ROM, 320KB SRAM, 16KB RTC SRAM
- Support UART / GPIO / ADC / PWM / SPI / I2C / LCD / I2S / Camera / IR / USB / DAC interface, support touch sensor, temperature sensor, pulse counter
- SMD-42 packaging
- Integrate Wi-Fi MAC/ BB/RF/PA/LNA
- Support multiple sleep modes, deep sleep current is less than10uA
- Serial port speed up to4Mbps

- Built-in Lwip protocol stack
- Support STA/AP/STA+AP work mode
- Smart Config (APP) / AirKiss (WeChat) one-click distribution network supporting Android and IOS
- Support serial local upgrade and remote firmware upgrade (FOTA)
- General AT command can be used quickly
- Support secondary development, integrated Windows, Linux development environment
- About PSRAM:

ESP-12K supports optional PSRAM, the default 2 kinds of PSRAM configuration, the shield can be distinguished on the silk screen. For details, please refer to the product appearance drawing.

ESP-12K(00) without PSRAM

ESP-12K(08) configuration 8MByte PSRAM

Main parameter

List 1 Main parameter

Model Name	ESP-12K
Packaging	SMD-42
Size	31.0*18.0*3.0(±0.2)MM
Antenna	PCB antenna/IPEX connector
Spectrum range	2400 ~ 2483.5MHz
Work Temperature	-40 ℃ ~ 85 ℃
Storage environment	-40 ℃ ~ 125 ℃，< 90%RH
Power Supply Range	Voltage 3.0V ~ 3.6V，Current >500mA

Interface	UART/GPIO/ADC/PWM/SPI/I2C/LCD/I2S/Camera/IR/USB/DAC
IO port qty	37
Serial rate	Support 110 ~ 4608000 bps ， default 115200 bps
Safety	WEP/WPA-PSK/WPA2-PSK
SPI Flash	Default 32Mbit
PSRAM	Optional without PSRAM or 8MByte PSRAM

2.ELECTRICAL PARAMETER

Parameter		Condition	Min	Typical	Max	Unit
Voltage		VDD	3.0	3.3	3.6	V
I/O	V_{IL}/V_{IH}	-	-0.3/0.75VIO	-	0.25VIO/3.6	V
	V_{OL}/V_{OH}	-	N/0.8VIO	-	0.1VIO/N	V
	I_{MAX}	-	-	-	12	mA

RF performance

Description	Typical	Unit
Work frequency	2400 - 2483.5	MHz
Output power		
In 11n mode HT40，PA output power is	12±2	dBm
In 11n mode HT20，PA output power is	13±2	dBm
In 11g mode，PA output power is	14±2	dBm
In 11b mode，PA output power is	16±2	dBm
Receive sensitivity		
CCK, 1 Mbps	<=-96	dBm
CCK, 11 Mbps	<=-88	dBm
6 Mbps (1/2 BPSK)	<=-91	dBm
54 Mbps (3/4 64-QAM)	<=-74	dBm
HT20 (MCS7)	<=-71	dBm
HT40 (MCS7)	<=-68	dBm

Power consumption

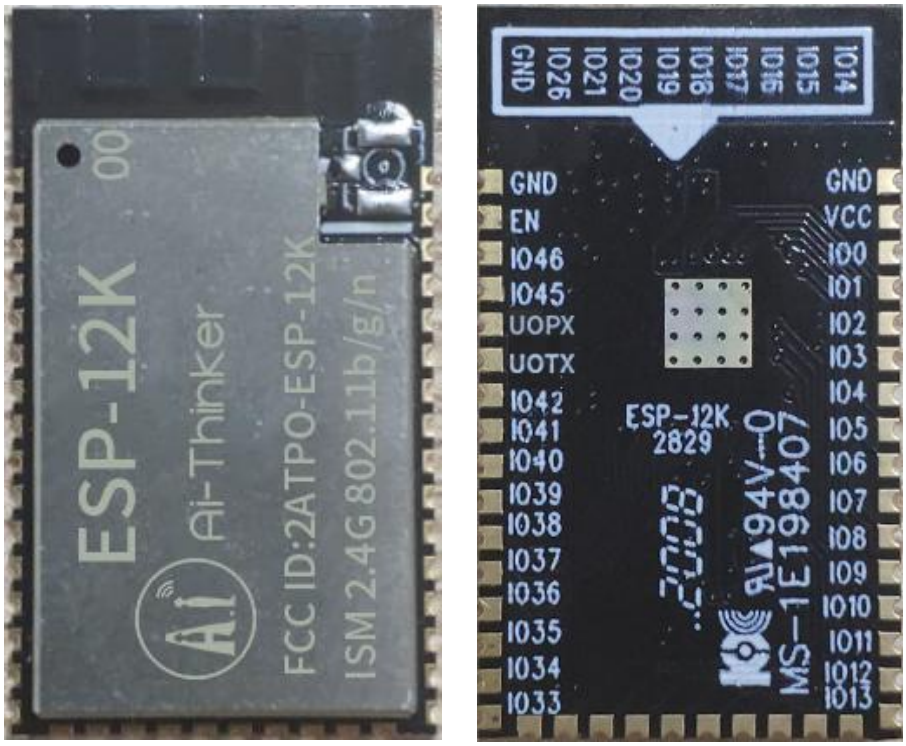
The following power consumption data is based on a 3.3V power supply, an ambient temperature of 25 ° C, and is measured using an internal voltage regulator.

- All measurements are done at the antenna interface without SAW filters.
- All transmission data is based on a 90% duty cycle, measured in continuous transmission mode.

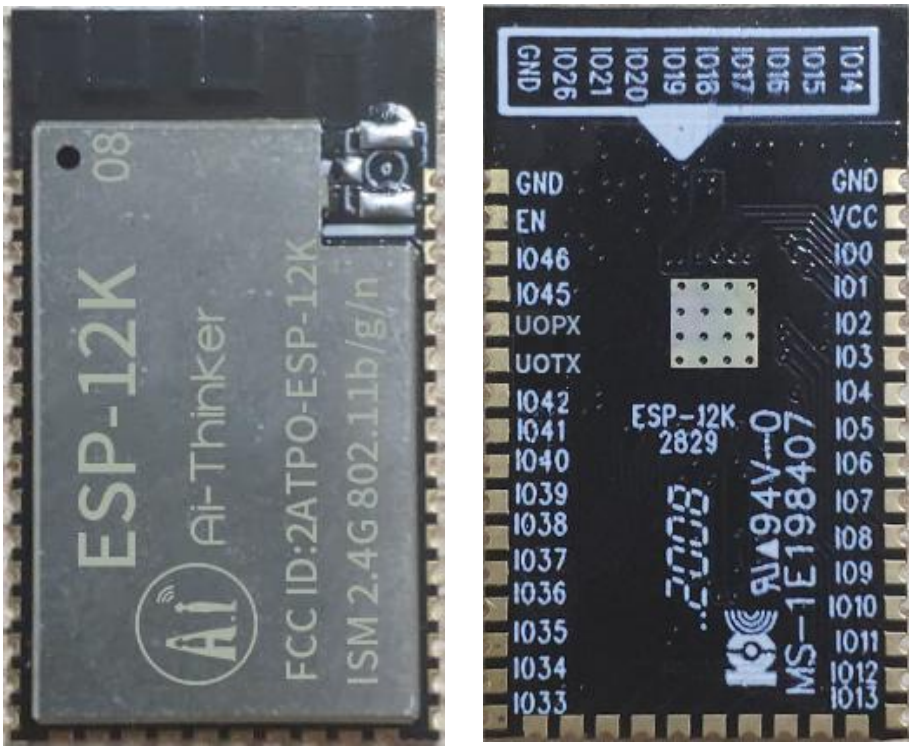
Mode	Mix	Typical	Max	Unit
Send 802.11b, CCK 11Mbps, POUT=+17dBm	-	190	-	mA
Send 802.11g, OFDM 54Mbps, POUT =+15dBm	-	145	-	mA
Send 802.11n, MCS7, POUT =+13dBm	-	120	-	mA
Receive 802.11b,package length 1024bit, -80dBm	-	63	-	mA
Receive 802.11g, package length 1024, -70dBm	-	63	-	mA
Receive 802.11n,package length 1024bit, -65dBm	-	68	-	mA
Modem-Sleep①	-	20	-	mA
Light-Sleep②	-	1.4	-	mA
Deep-Sleep③	-	20	-	μA
Power Off	-	0.5	-	μA

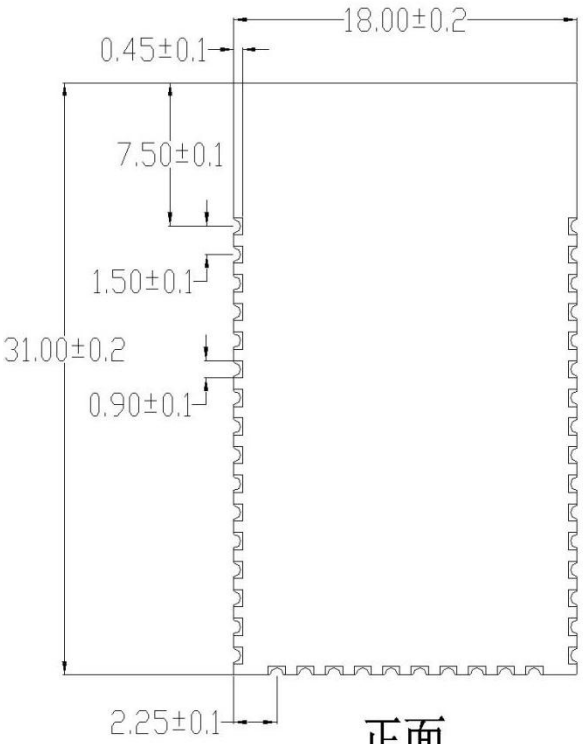
3.DIMENSION

ESP-12K（00）

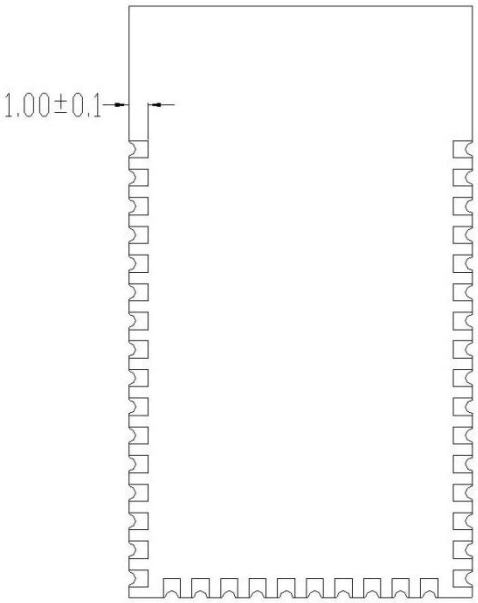


ESP-12K（08）





正面



背面

4.PIN DEFINITION

The ESP-12K module has a total of 42 interfaces, such as the pin diagram, the pin function definition table is the interface definition

ESP-12K PIN definition diagram

List PIN function definition

No.	item	Function Description
1	GND	ground
2	VCC	Power supply
3	IO0	RTC_GPIO0, GPIO0
4	IO1	RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0
5	IO2	RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1
6	IO3	RTC_GPIO3, GPIO3, TOUCH3, ADC1_CH2
7	IO4	RTC_GPIO4, GPIO4, TOUCH4, ADC1_CH3
8	IO5	RTC_GPIO5, GPIO5, TOUCH5, ADC1_CH4
9	IO6	RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5

10	IO7	RTC_GPIO7, GPIO7, TOUCH7, ADC1_CH6
11	IO8	RTC_GPIO8, GPIO8, TOUCH8, ADC1_CH7
12	IO9	RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, FSPIHD
13	IO10	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPICS0, FSPIIO4
14	IO11	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPID, FSPIIO5
15	IO12	RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPICLK, FSPIIO6
16	IO13	RTC_GPIO13, GPIO13, TOUCH13, ADC2_CH2, FSPIQ, FSPIIO7
17	IO14	RTC_GPIO14, GPIO14, TOUCH14, ADC2_CH3, FSPIWP, FSPIDQS
18	IO15	RTC_GPIO15, GPIO15, U0RTS, ADC2_CH4, XTAL_32K_P
19	IO16	RTC_GPIO16, GPIO16, U0CTS, ADC2_CH5, XTAL_32K_N
20	IO17	RTC_GPIO17, GPIO17, U1TXD, ADC2_CH6, DAC_1
21	IO18	RTC_GPIO18, GPIO18, U1RXD, ADC2_CH7, DAC_2, CLK_OUT3
22	IO19	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, USB_D-
23	IO20	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, USB_D+
24	IO21	RTC_GPIO21, GPIO21
25	IO26	SPICS1, GPIO26
26	GND	接地
27	IO33	SPIIO4, GPIO33, FSPIHD
28	IO34	SPIIO5, GPIO34, FSPICS0
29	IO35	SPIIO6, GPIO35, FSPID
30	IO36	SPIIO7, GPIO36, FSPICLK
31	IO37	SPIDQS, GPIO37, FSPIQ
32	IO38	GPIO38, FSPIWP

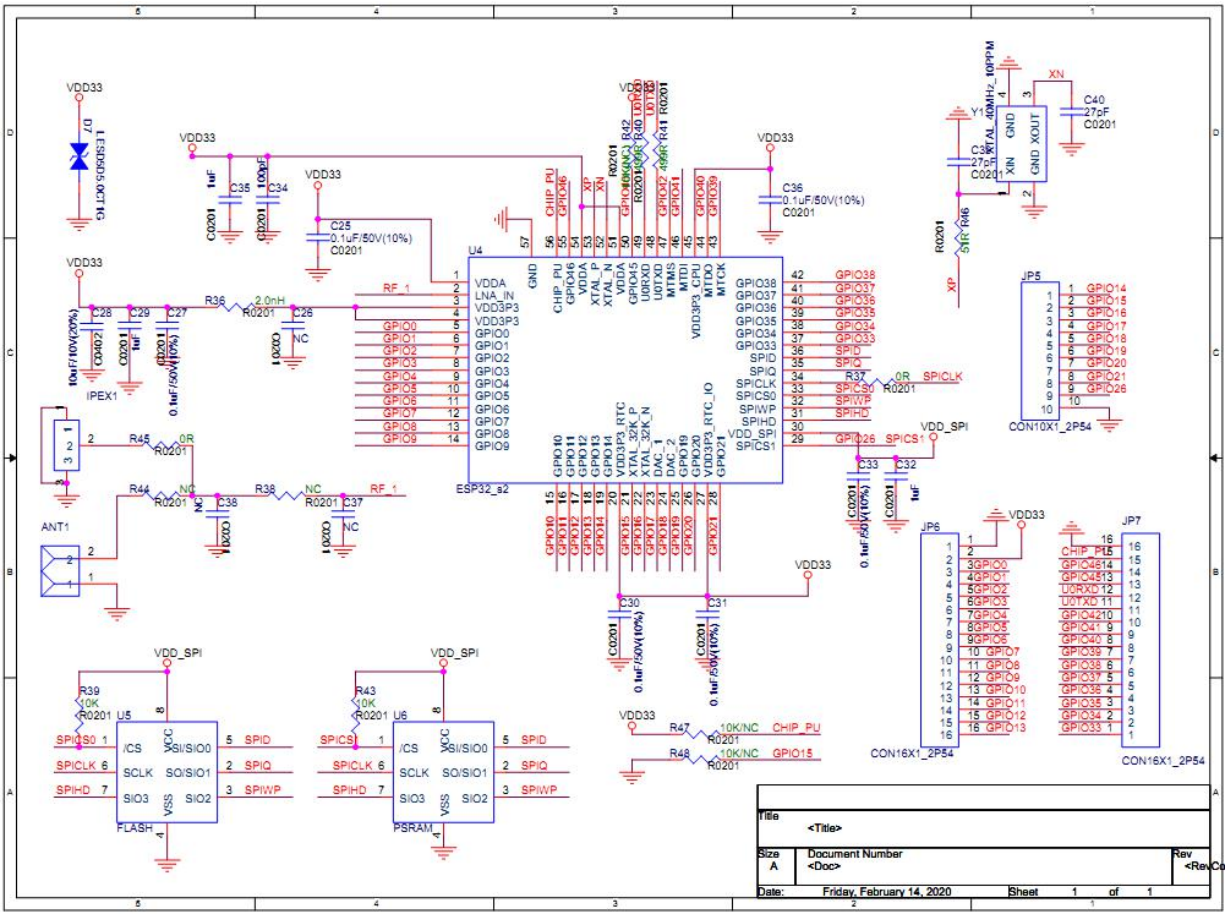
33	IO39	MTCK, GPIO39, CLK_OUT3
34	IO40	MTDO, GPIO40, CLK_OUT2
35	IO41	MTDI, GPIO41, CLK_OUT1
36	IO42	MTMS, GPIO42
37	U0TX	U0TXD, GPIO43, CLK_OUT1
38	U0RX	U0RXD, GPIO44, CLK_OUT2
39	IO45	GPIO45
40	IO46	GPIO46
41	EN	High level: chip enable; Low level: the chip is off; Has been raised by default.
42	GND	Ground

List Module startup mode description

System startup mode			
Pin	Default	SPI startup mode	Download startup mode
IO0	Pull up	1	0
IO46	Pull down	Irrelevant	0

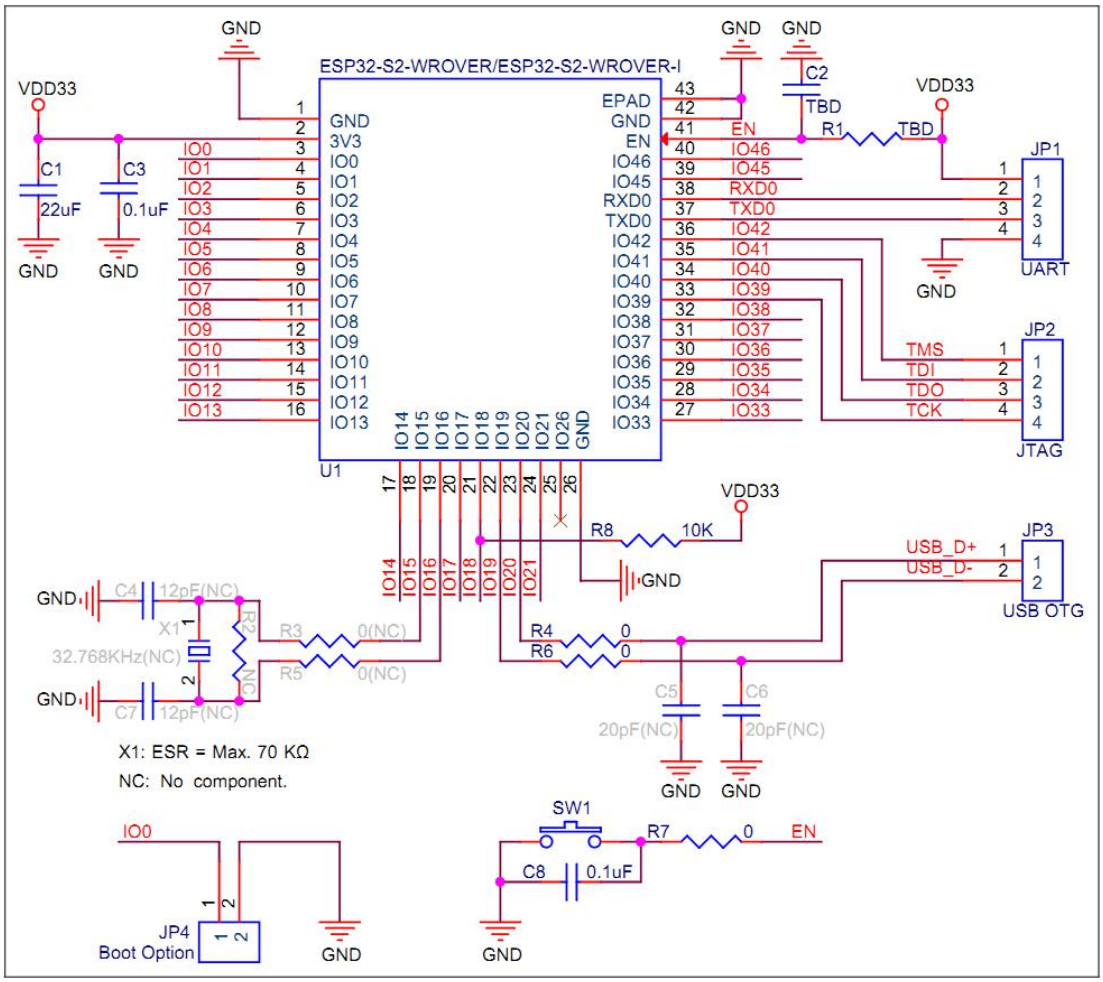
Note: Some pins have been pulled up internally, please refer to the schematic

5.SCHEMATIC DIAGRAM



6.DESIGN GUIDE

1、Application circuit



note:

(1) The RC delay circuit needs to be added to the EN pin. It is recommended that R = 10kΩ and C = 0.1μF;

(2) GPIO18 as U1RXD needs to add a pull-up resistor externally.

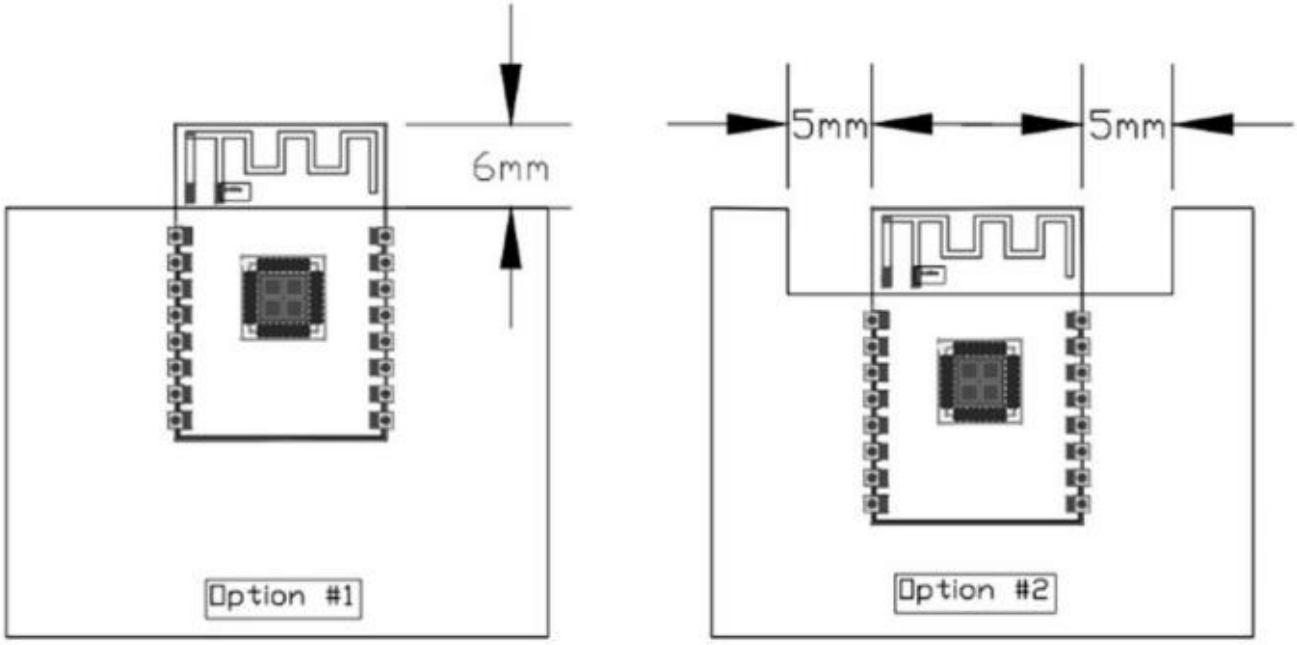
2、Antenna layout requirements

(1) The following two methods are recommended for the installation location on the motherboard:

Option 1: Place the module on the edge of the main board, and the antenna area protrudes from the edge of the main board.

Option 2: Place the module on the edge of the motherboard, and the edge of the motherboard digs out an area at the position of the antenna.

(2) In order to meet the performance of the onboard antenna, it is forbidden to place metal parts around the antenna, away from high-frequency devices.



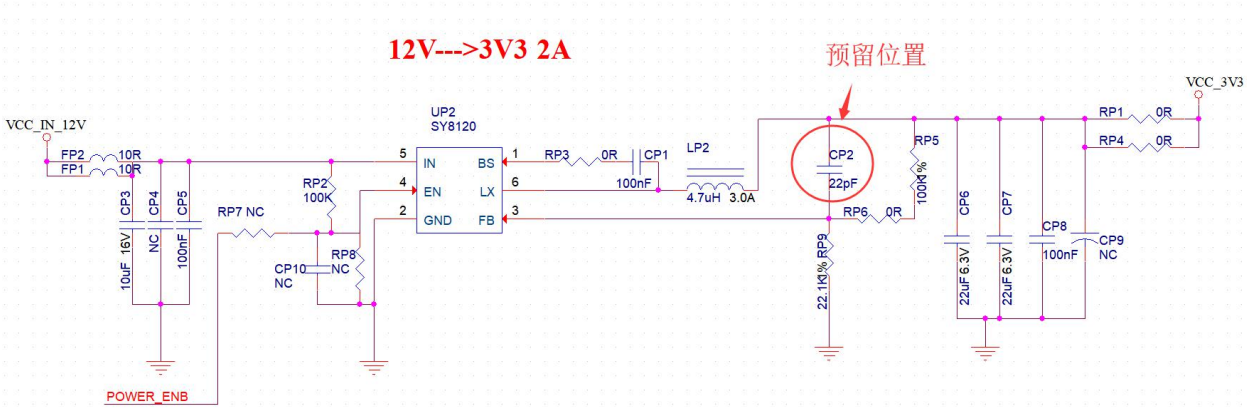
3、Power supply

(1) 3.3V voltage is recommended, the peak current is more than 500mA

(2) It is recommended to use LDO for power supply; if using DC-DC, it is recommended to control the ripple within 30mV.

(3) It is recommended to reserve the position of the dynamic response capacitor in the DC-DC power supply circuit, which can optimize the output ripple when the load changes greatly.

(4), 3.3V power interface is recommended to add ESD devices.



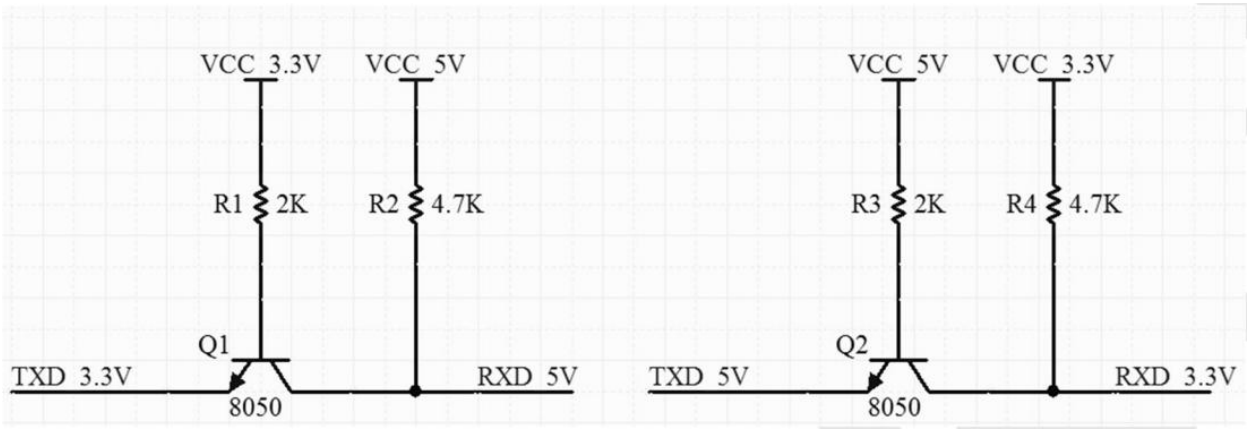
4、Use of GPIO port

(1) Some GPIO ports are led out of the periphery of the module. If you need to use a 10-100 ohm resistor in series with the IO port. This can suppress overshoot, and the level on both sides is more stable. Helps both EMI and ESD.

(2) For the up and down of the special IO port, please refer to the instruction manual of the specification, which will affect the startup configuration of the module.

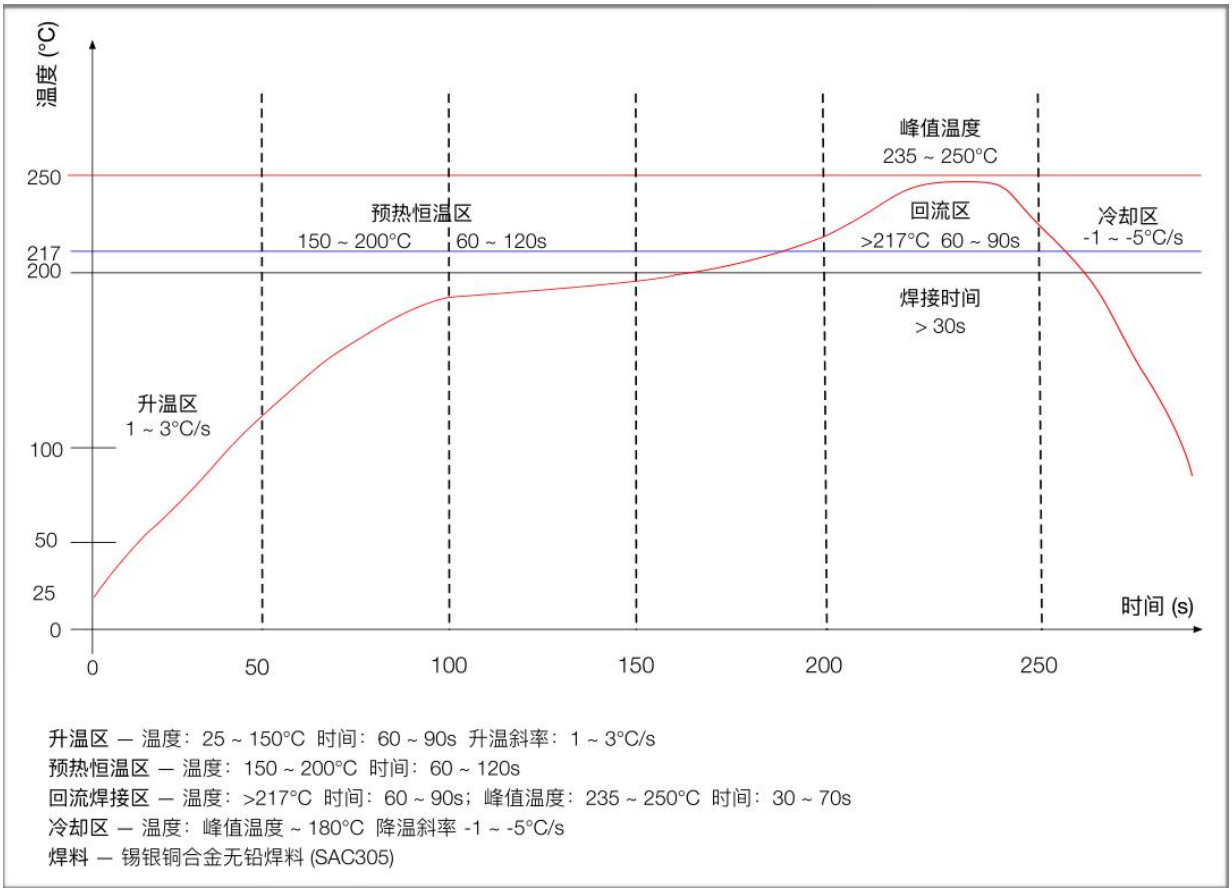
(3) The IO port of the module is 3.3V. If the IO level of the main control and the module does not match, a level conversion circuit needs to be added.

(4) If the IO port is directly connected to the peripheral interface, or the pin header and other terminals, it is recommended to reserve ESD devices near the terminal of the IO trace.



Pic Level shift circuit

7.RRFLOW SOLDERING CURER



升温区 — 温度：25 ~ 150°C 时间：60 ~ 90s 升温斜率：1 ~ 3°C/s
预热恒温区 — 温度：150 ~ 200°C 时间：60 ~ 120s
回流焊接区 — 温度：>217°C 时间：60 ~ 90s；峰值温度：235 ~ 250°C 时间：30 ~ 70s
冷却区 — 温度：峰值温度 ~ 180°C 降温斜率 -1 ~ -5°C/s
焊料 — 锡银铜合金无铅焊料 (SAC305)

8.PACKAGING

As shown below, the packaging of ESP-12K is taping.

9.CONTACT US

Website：https://www.ai-thinker.com

Development DOCS：https://docs.ai-thinker.com

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